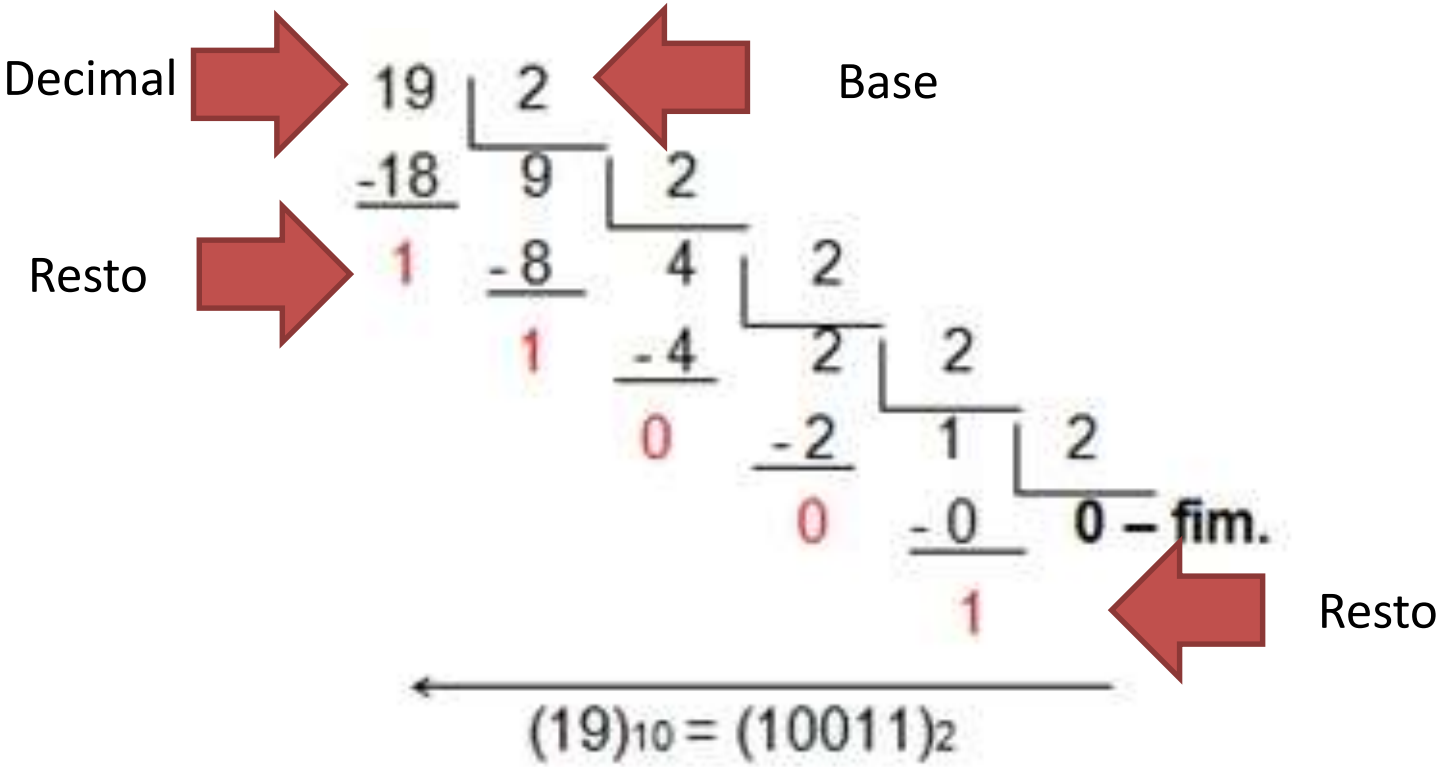
QUARTUS 9 SP2
AULA 2 PARTE 1

Monitoria de Sistemas Digitais

04/12/13

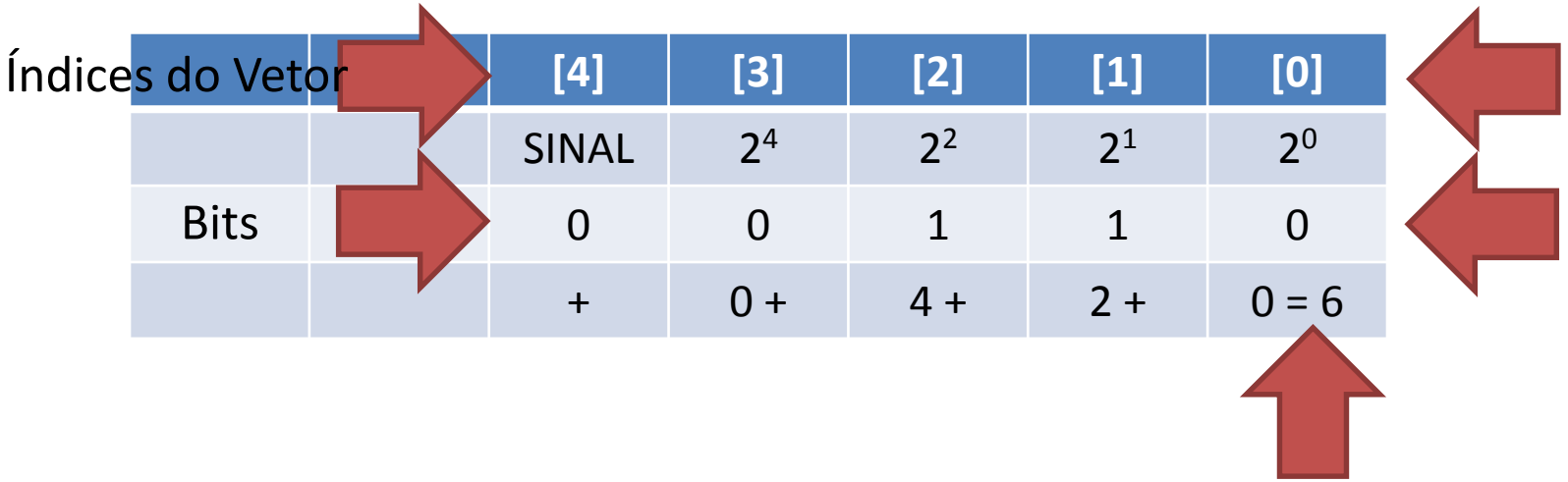
Vetores

- Número Decimal para Binário
  - Resto das divisões sucessivas



Vetores

- Número Binário para Decimal
  - Resto das divisões sucessivas



Índices do Vetor		[4]	[3]	[2]	[1]	[0]
		SINAL	2^4	2^2	2^1	2^0
Bits		0	0	1	1	0
		+	0 +	4 +	2 +	0 = 6

$(0110)_2 = 0_{(3)}1_{(2)}1_{(1)}0_{(0)}$

Decimal

0*2^3 + 1*2^2 + 1*2^1 +0*2^0 = 0 + 1*4 + 1*2 + 0 = 4 + 2 = $(6)_{10}$[2]

Vetores

- Número Binário para Decimal
  - Representação do Sinal

Quem define é você
Mas todo número tem sinal!

		[4]	[3]	[2]	[1]	[0]
		SINAL	2^4	2^2	2^1	2^0
		1	0	1	1	0
		-	0 +	4 +	2 +	0 = - 6

$(0110)_2 = 0_{(3)}1_{(2)}1_{(1)}0_{(0)}$

$0*2^3 + 1*2^2 + 1*2^1 + 0*2^0 = 0 + 1*4 + 1*2 + 0 = 4 + 2 = (-6)_{10}$[2]

Vetores

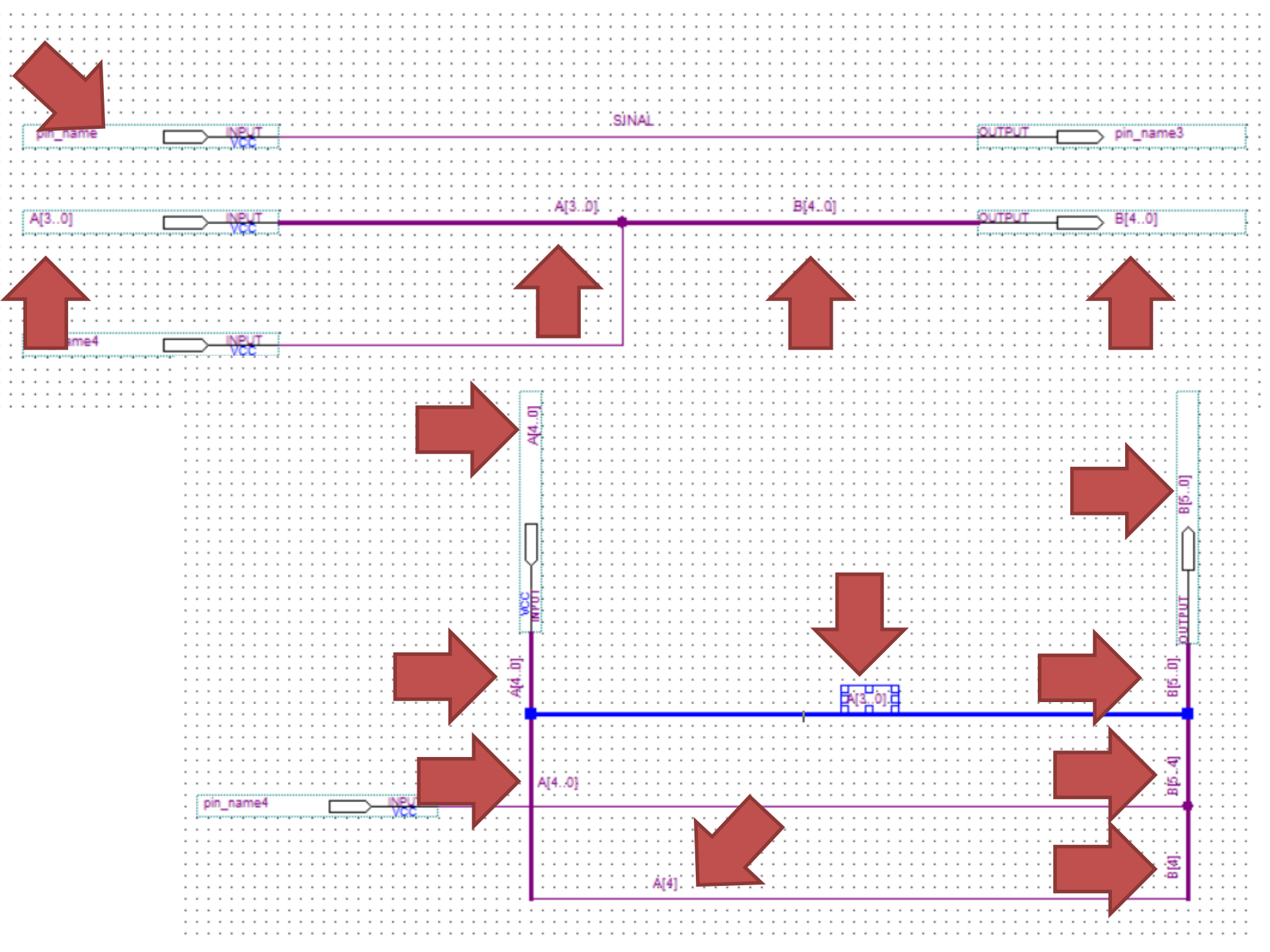
- Número Binário para Decimal
  - Número maior?

Quem define é você

	[5]	[4]	[3]	[2]	[1]	[0]
	SINAL	2^5	2^4	2^2	2^1	2^0
	1	1	0	1	1	0
	-	16	0 +	4 +	2 +	0 = - 22

$(0110)_2 = 0_{(3)}1_{(2)}1_{(1)}0_{(0)}$

$0*2^3 + 1*2^2 + 1*2^1 + 0*2^0 = 0 + 1*4 + 1*2 + 0 = 4 + 2 = (-6)_{10}$[2]


pin_name
INPUT
VCC
SINAL
OUTPUT
pin_name3
A[3..0]
INPUT
VCC
A[3..0]
B[4..0]
OUTPUT
B[4..0]
INPUT
VCC
A[4..0]
VCC
INPUT
A[4..0]
A[3..0]
B[5..0]
OUTPUT
B[5..0]
pin_name4
INPUT
VCC
A[4..0]
B[5..4]
A[4]
B[4]

Todo número tem sinal?

Vetores

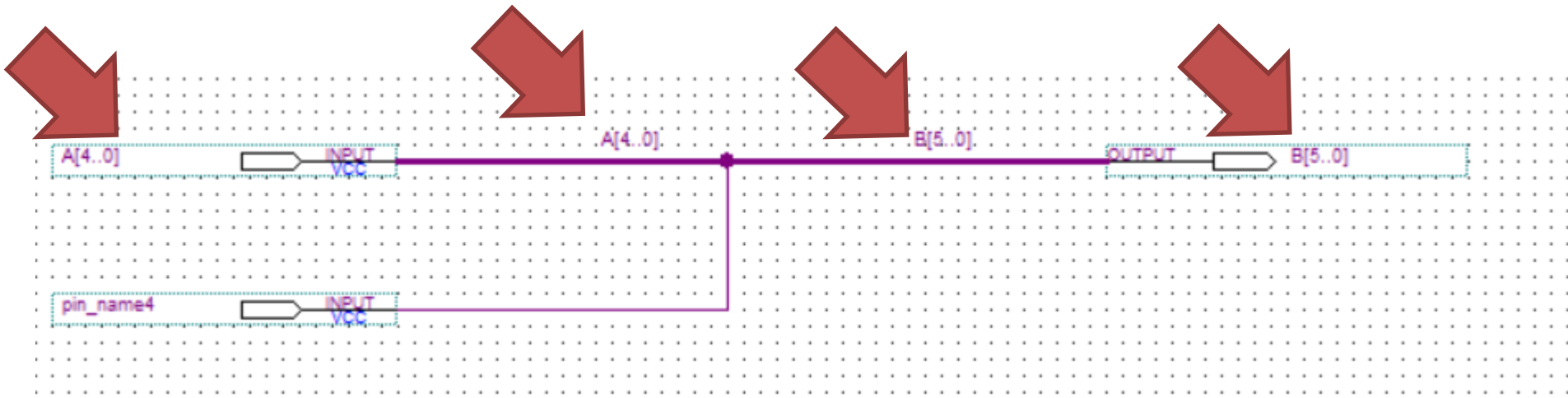
- Melhor organizando
  - Sinal a parte

Sinal!
Tratado em separado

	[5]	[4]	[3]	[2]	[1]	[0]
	2^n...	2^3	2^2	2^1	2^0	SINAL
	1	0	1	1	0	1
	$1*2^n$ +	0 +	4 +	2 +	0 = -6	

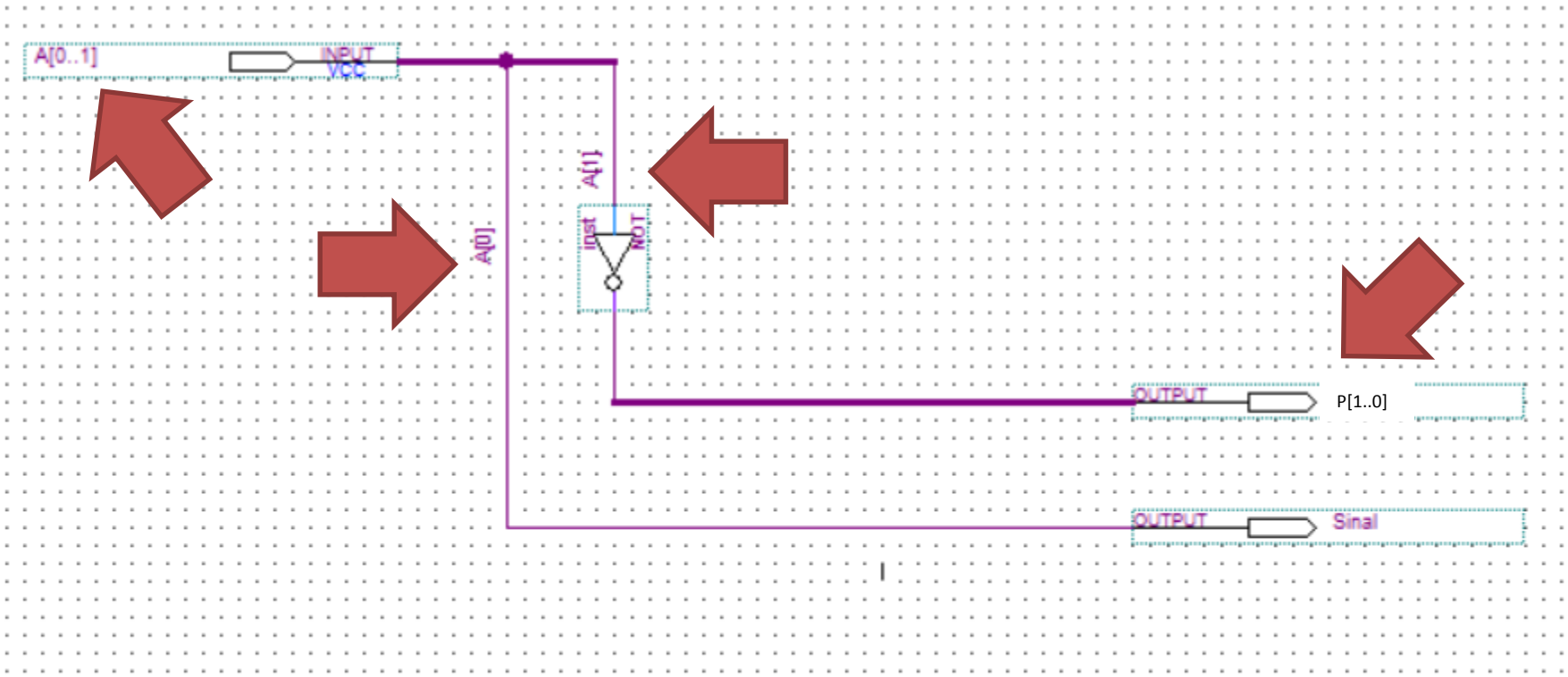
$(0110)_2 = 0_{(3)}1_{(2)}1_{(1)}0_{(0)}$

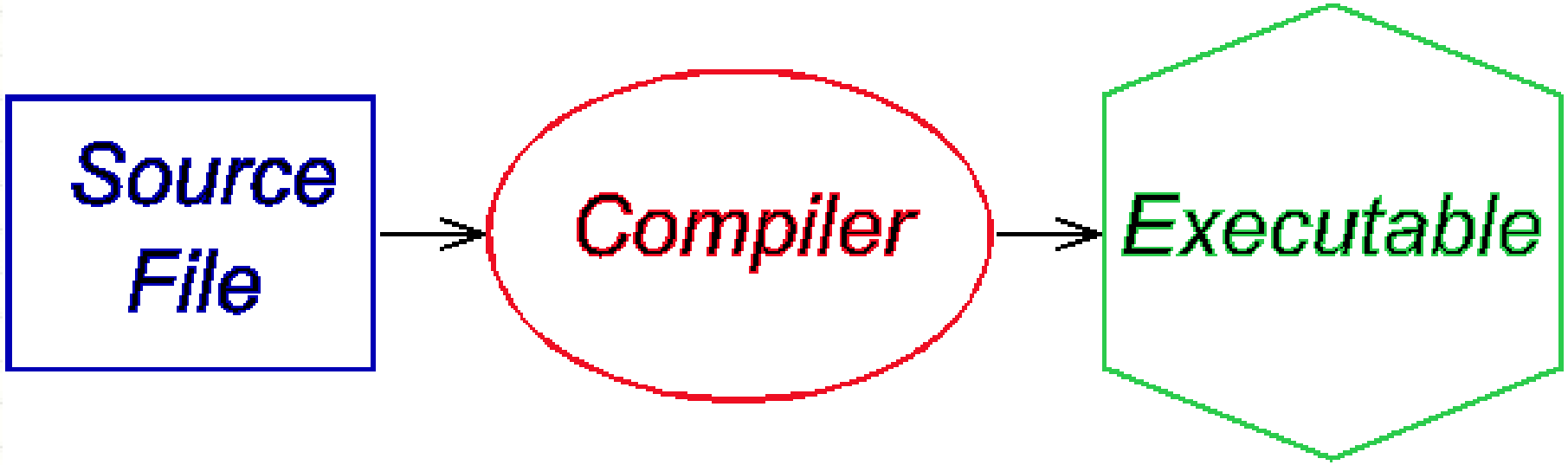
$0*2^3 + 1*2^2 + 1*2^1 + 0*2^0 = 0 + 1*4 + 1*2 + 0 = 4 + 2 = (-6)_{10}$[2]


A[4..0]
INPUT
VCC
A[4..0]
B[5..0]
OUTPUT
B[5..0]
pin_name4
INPUT
VCC

Exercício 1:

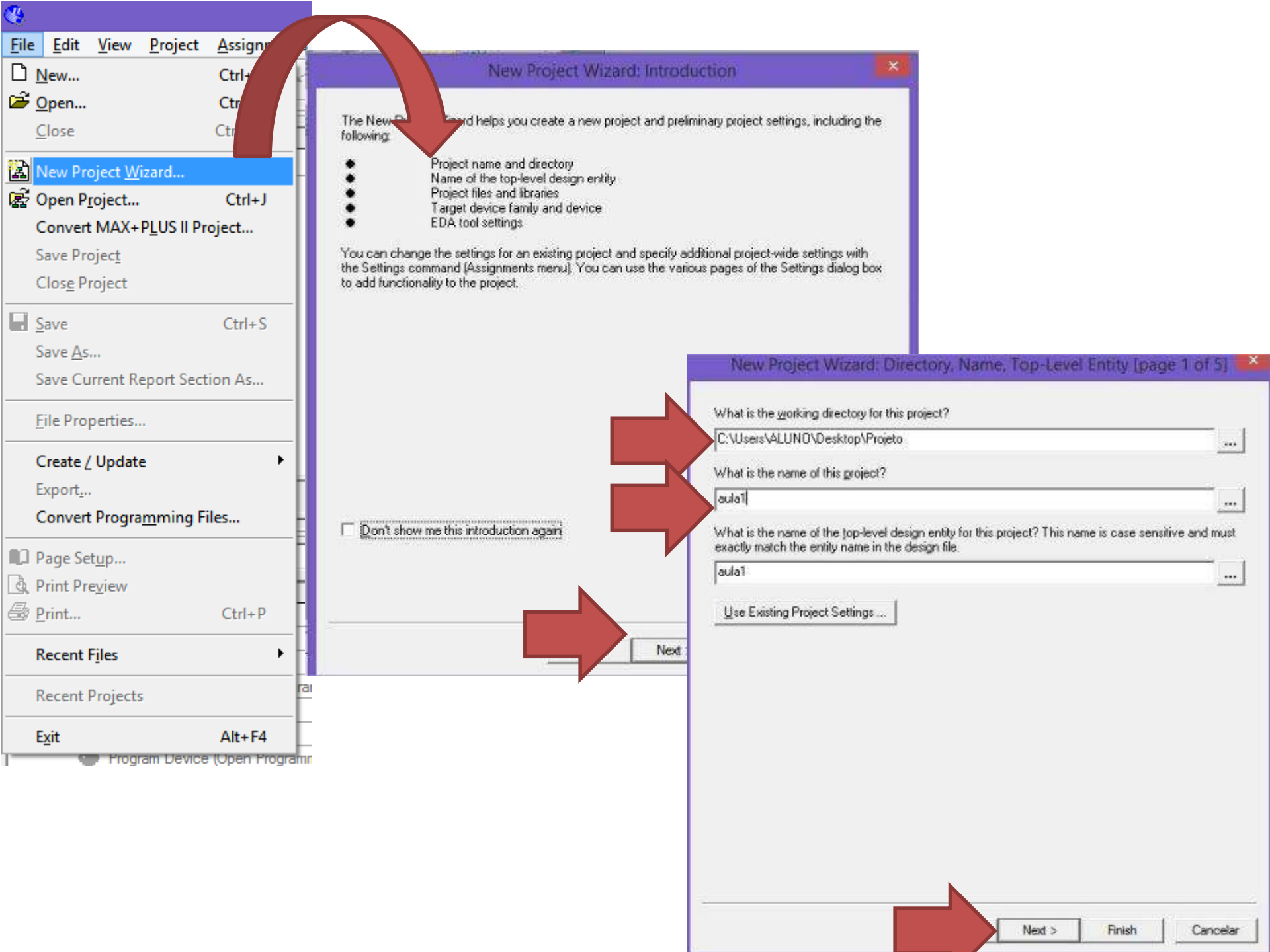
- Criar por vetor, utilize BDF
  - IN:
    - Vetor que representa de + 1 até -1.
  - LOGICA:
    - Inverta o valor de cada bit do módulo (exceto o sinal).
  - OUT:
    - Vetor que possa representar de +3 até -3
    - Sinal em “fio” separado.


A[0..1]
INPUT
VCC
A[1]
A[0]
inst
NOT
OUTPUT
P[1..0]
OUTPUT
Sinal

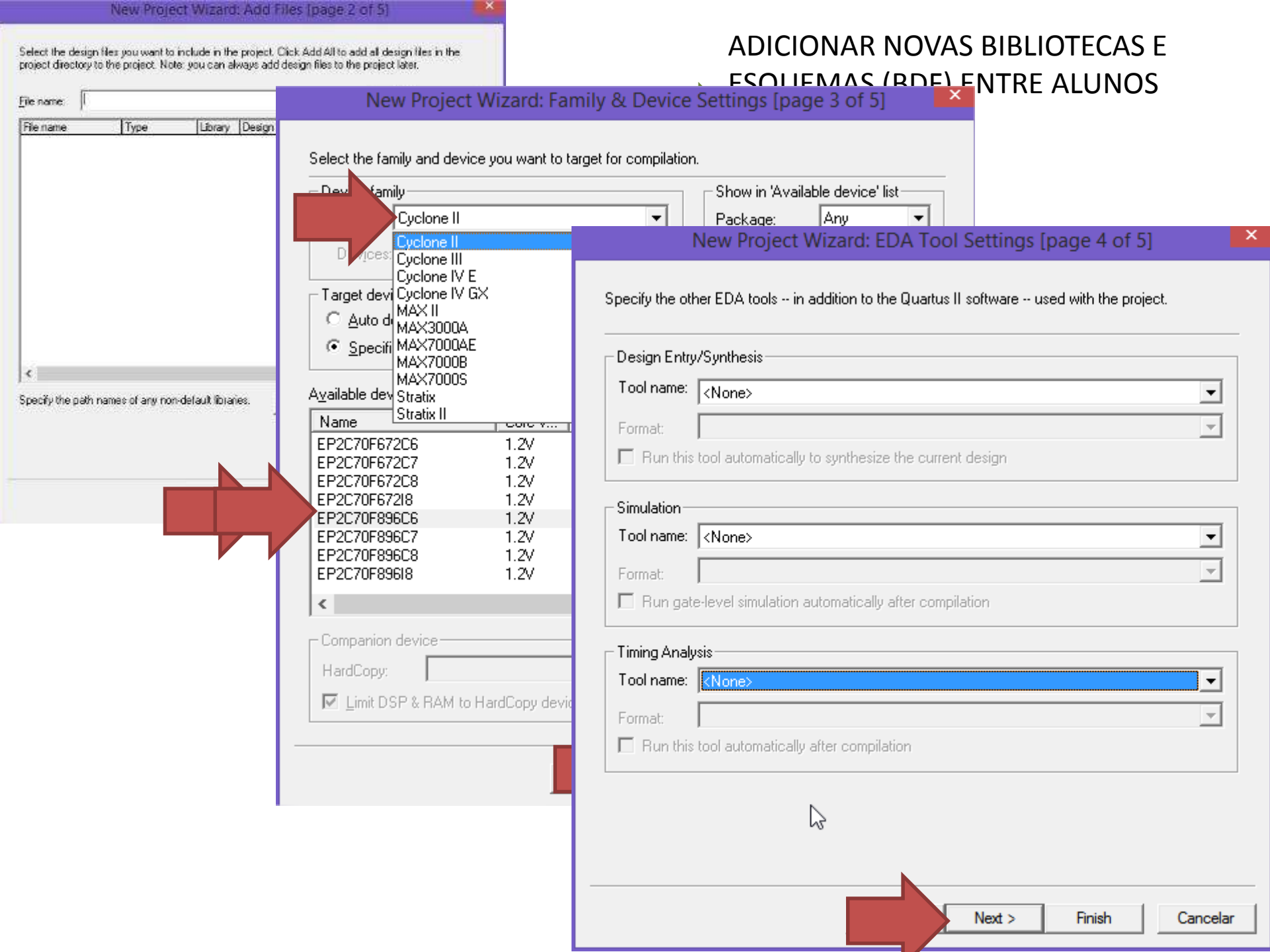


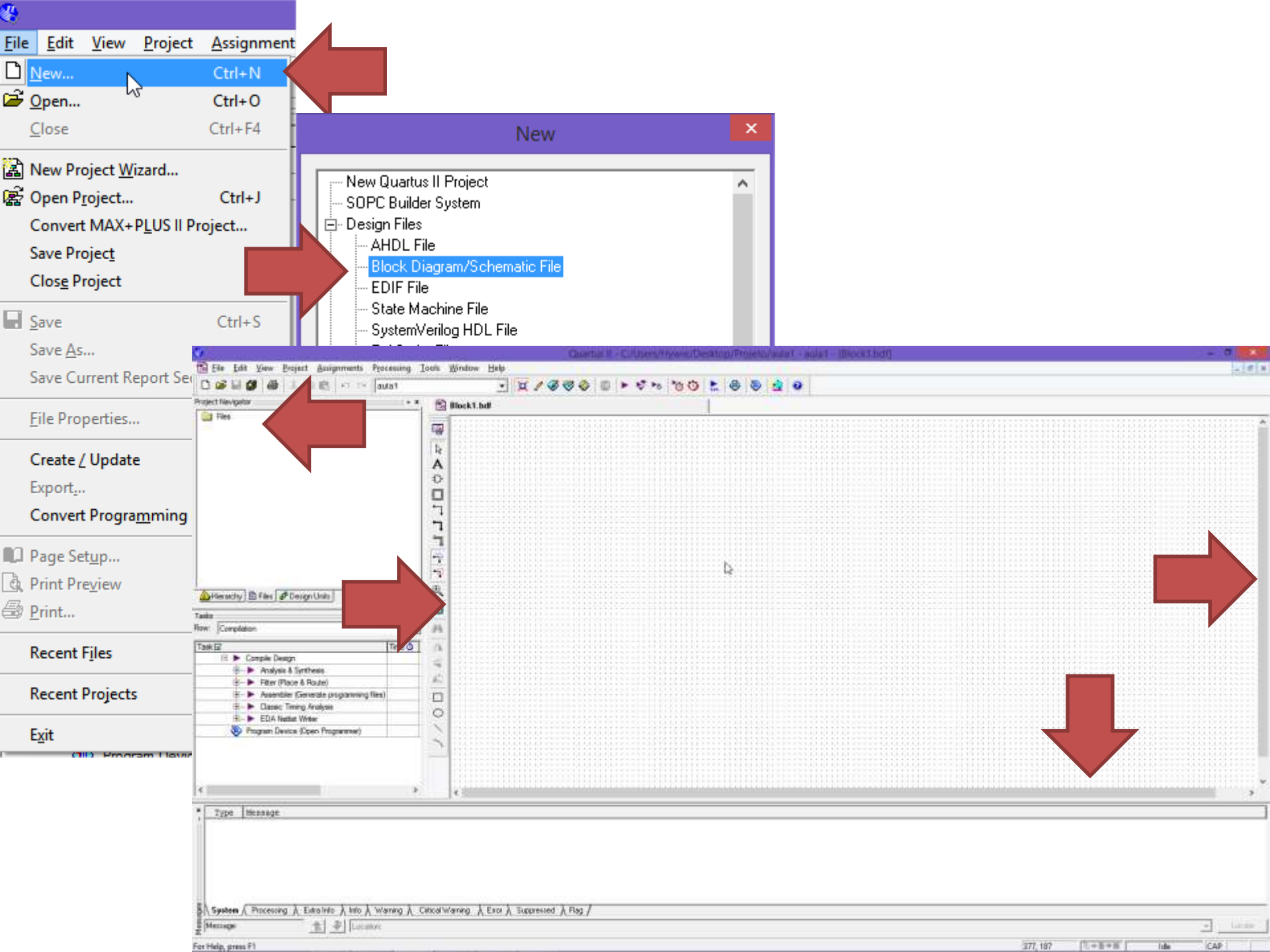
Parte 2: Compilando!

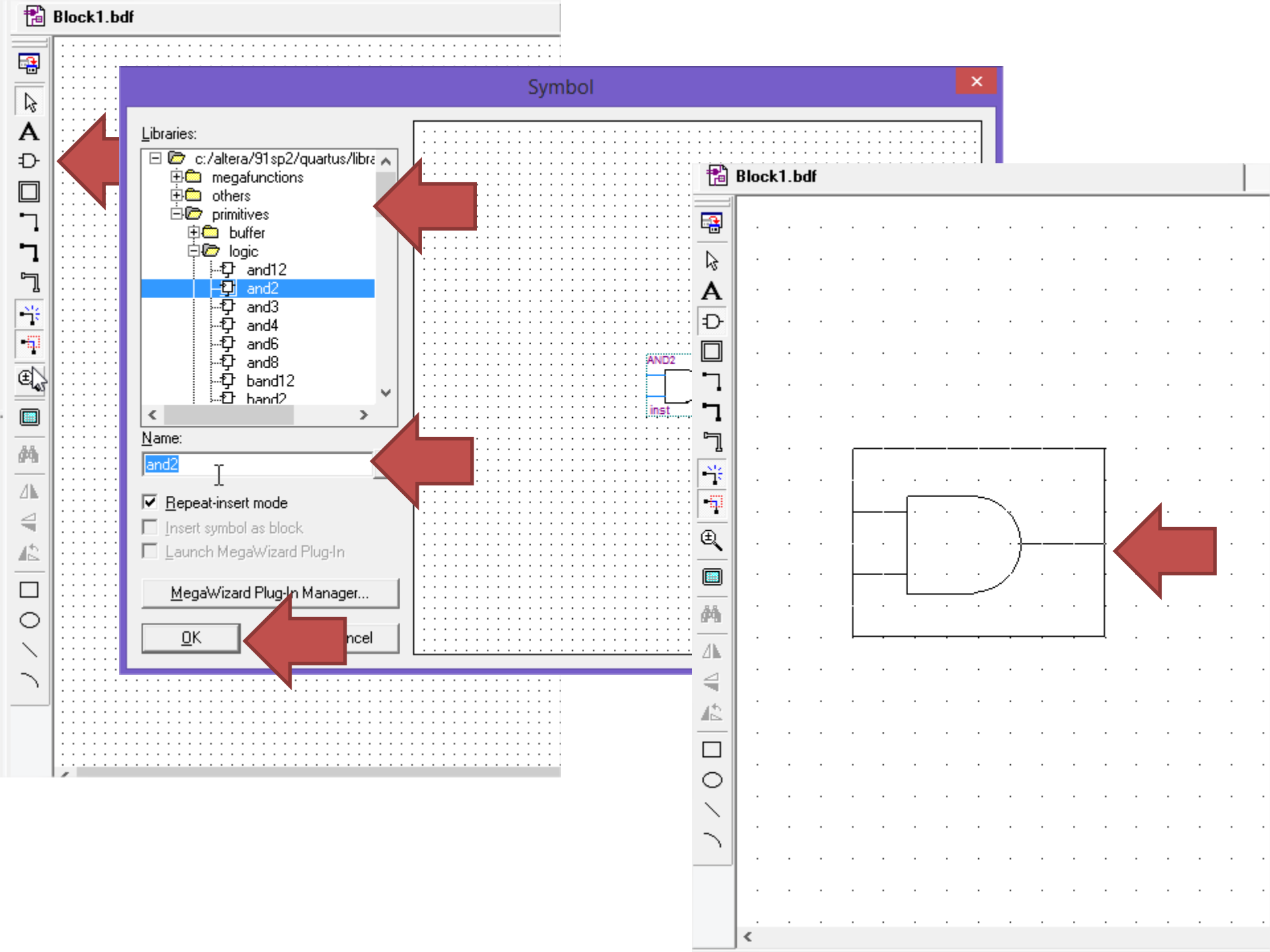
1. Construir por BDF
    1. (A ^ B) : AND2 (compilar)

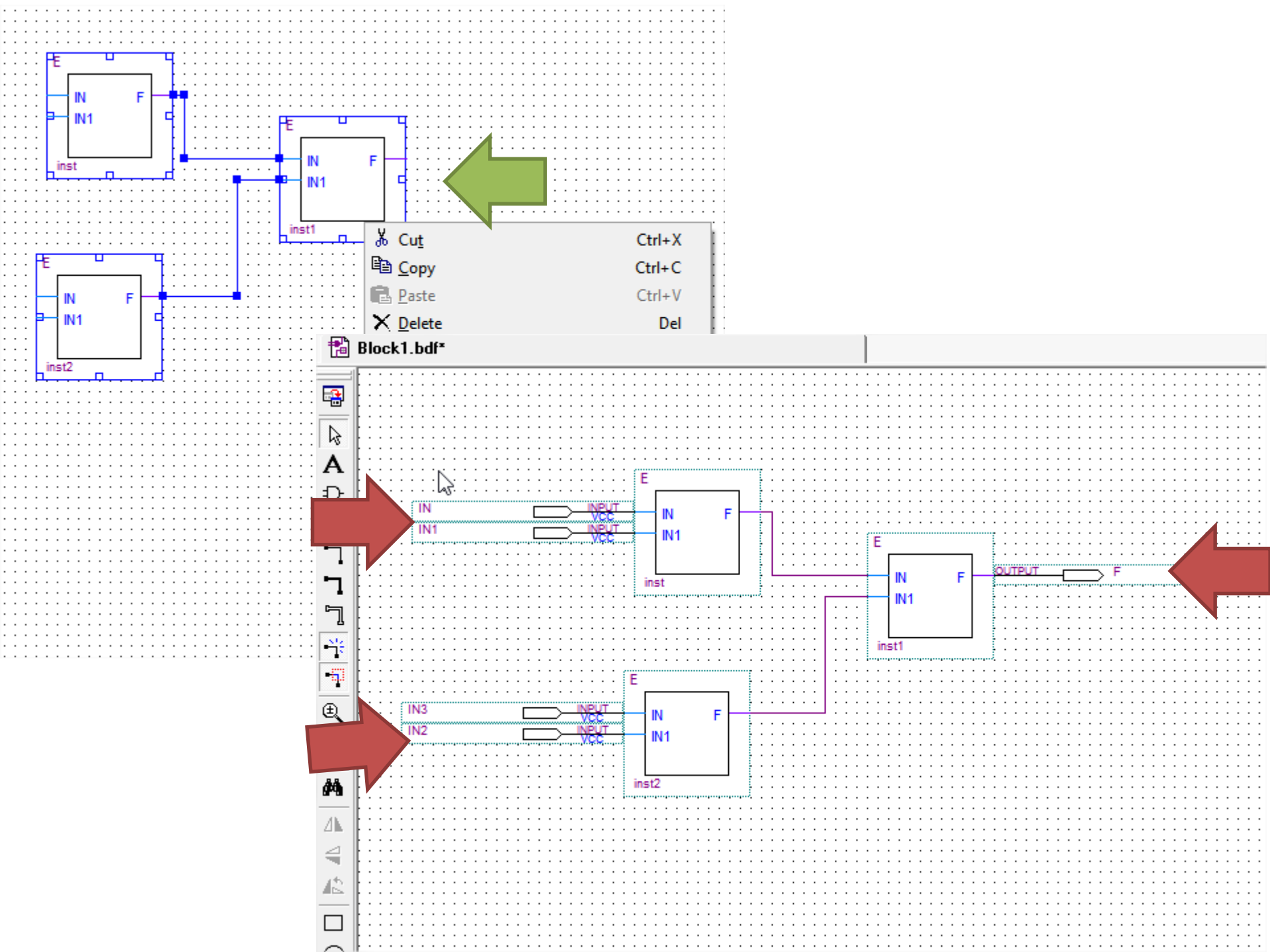

File
Edit
View
Project
New...
Open...
Close
New Project Wizard...
Open Project... Ctrl+J
Convert MAX+PLUS II Project...
Save Project
Close Project
Save Ctrl+S
Save As...
Save Current Report Section As...
File Properties...
Create / Update
Export...
Convert Programming Files...
Page Setup...
Print Preview
Print... Ctrl+P
Recent Files
Recent Projects
Exit Alt+F4
New Project Wizard: Introduction
The New Project Wizard helps you create a new project and preliminary project settings, including the following:
Project name and directory
Name of the top-level design entity
Project files and libraries
Target device family and device
EDA tool settings
You can change the settings for an existing project and specify additional project-wide settings with the Settings command (Assignments menu). You can use the various pages of the Settings dialog box to add functionality to the project.
Don't show me this introduction again
Next
New Project Wizard: Directory, Name, Top-Level Entity [page 1 of 5]
What is the working directory for this project?
C:\Users\ALUNO\Desktop\Projeto
What is the name of this project?
aula1
What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.
aula1
Use Existing Project Settings ...
Next >
Finish
Cancelar

ADICIONAR NOVAS BIBLIOTECAS E ESQUEMAS (BDF) ENTRE ALUNOS

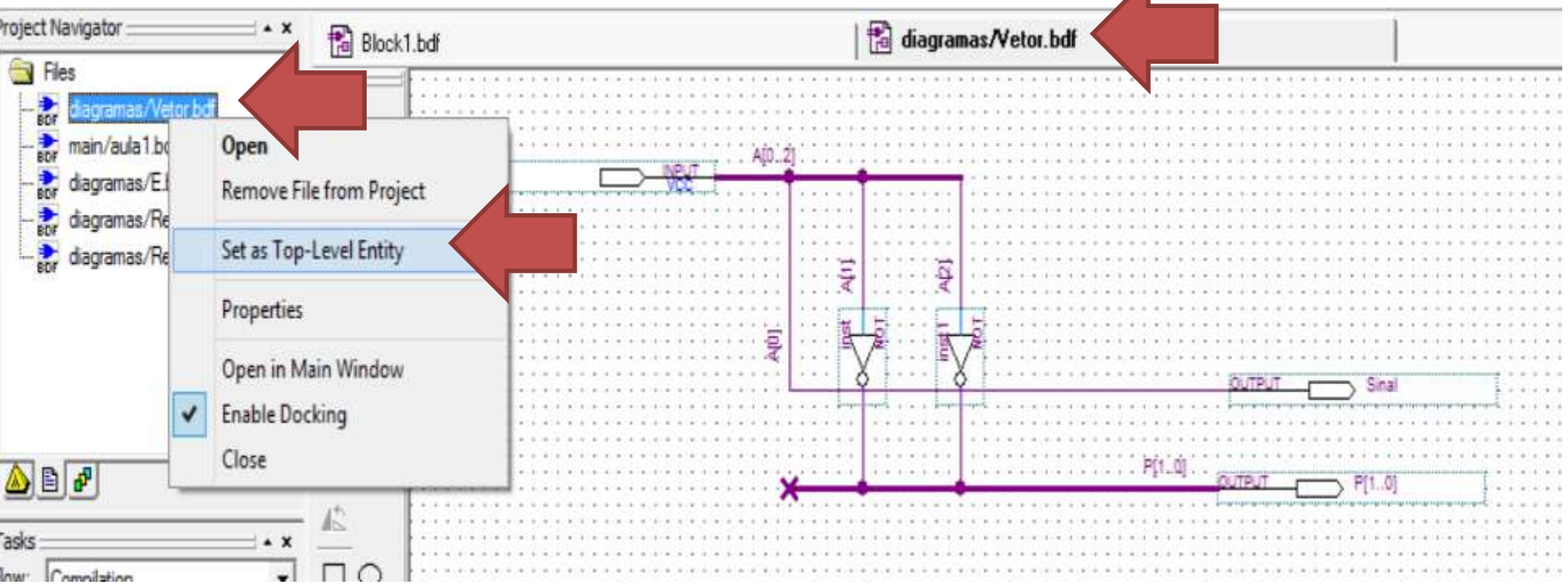


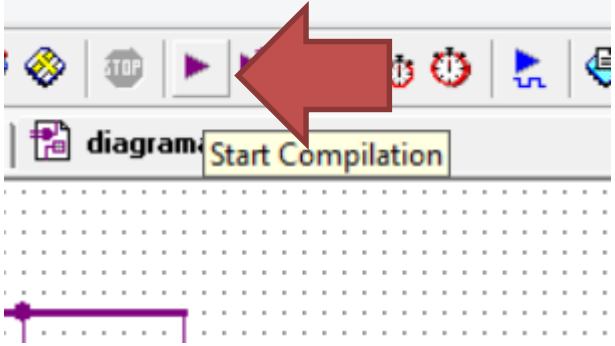

File
Edit
View
Project
Assignment
New... Ctrl+N
Open... Ctrl+O
Close Ctrl+F4
New Project Wizard...
Open Project... Ctrl+J
Convert MAX+PLUS II Project...
Save Project
Close Project
Save Ctrl+S
Save As...
Save Current Report Se
File Properties...
Create / Update
Export...
Convert Programming
Page Setup...
Print Preview
Print...
Recent Files
Recent Projects
Exit
New
New Quartus II Project
SOPC Builder System
Design Files
AHDL File
Block Diagram/Schematic File
EDIF File
State Machine File
SystemVerilog HDL File

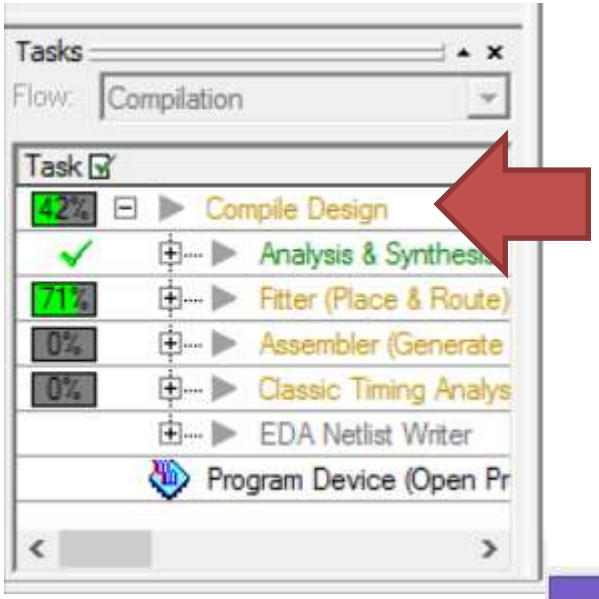

Block1.bdf
Symbol
Libraries:
c:/altera/91sp2/quartus/libra
megafunctions
others
primitives
buffer
logic
and12
and2
and3
and4
and6
and8
band12
hand2
Name:
and2
Repeat-insert mode
Insert symbol as block
Launch MegaWizard Plug-In
MegaWizard Plug-In Manager...
OK
ncel
AND2
inst
Block1.bdf

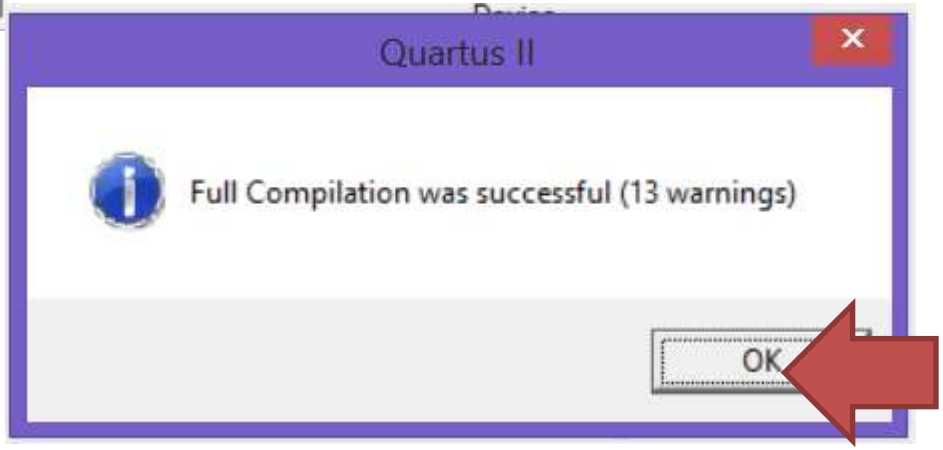

IN
IN1
F
inst
inst1
inst2
Cut Ctrl+X
Copy Ctrl+C
Paste Ctrl+V
Delete Del
Block1.bdf*
IN
IN1
INPUT
VCC
IN3
IN2
OUTPUT

Agora sim : Compilando...


Project Navigator
Files
diagramas/Vetor.bdf
main/aula1.bd
diagramas/E
diagramas/Re
diagramas/Re
Open
Remove File from Project
Set as Top-Level Entity
Properties
Open in Main Window
Enable Docking
Close
Block1.bdf
diagramas/Vetor.bdf
A[0..2]
A[1]
A[2]
A[0]
inst
inst1
NOT
NOT
OUTPUT
Sinal
P[1..0]
OUTPUT
P[1..0]
Tasks


Start Compilation


Tasks
Flow: Compilation
Task
42% Compile Design
Analysis & Synthesis
71% Fitter (Place & Route)
0% Assembler (Generate
0% Classic Timing Analys
EDA Netlist Writer
Program Device (Open Pr


Quartus II
Full Compilation was successful (13 warnings)
OK

Block1.bdf

Compilation Report - Flow Summary

- Compilation Report
  - Legal Notice
  - Flow Summary
  - Flow Settings
  - Flow Non-Default Global Se
  - Flow Elapsed Time
  - Flow OS Summary
  - Flow Log
  - Analysis & Synthesis
  - Fitter
  - Assembler
  - Timing Analyzer

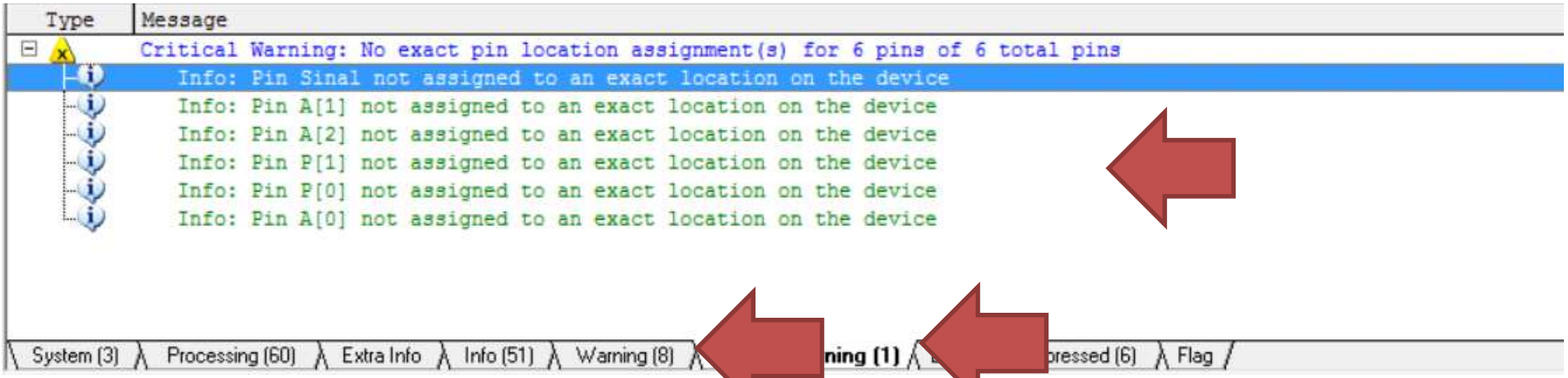
Flow Summary

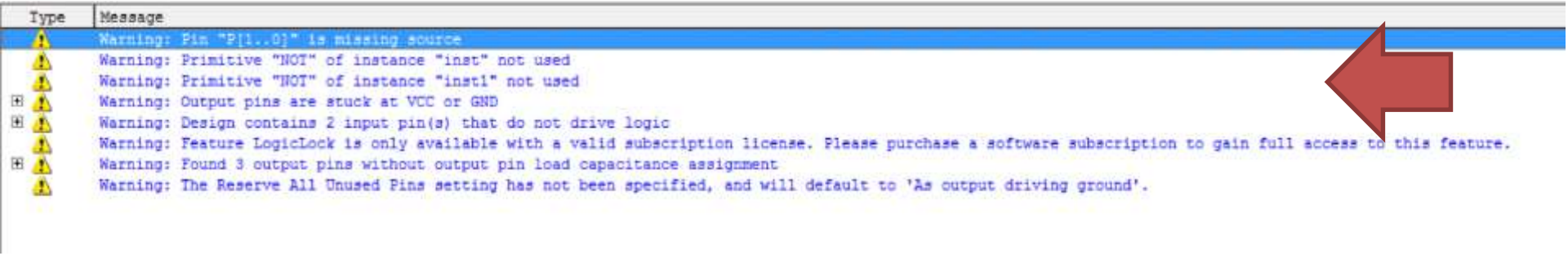
Flow Status	Successful - Tue Dec 03 00:08:53 2013
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	aula1
Top-level Entity Name	Vetor
Family	Cyclone II
Device	EP2C70F896C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	0 / 68,416 (0 %)
Total combinational functions	0 / 68,416 (0 %)
Dedicated logic registers	0 / 68,416 (0 %)
Total registers	0
Total pins	6 / 622 (< 1 %)

- Compilation Report
  - Legal Notice
  - Flow Summary
  - Flow Settings
  - Flow Non-Default Global Se
  - Flow Elapsed Time
  - Flow OS Summary
  - Flow Log
  - Analysis & Synthesis
  - Fitter
  - Assembler
  - Timing Analyzer
    - Summary
    - Settings
    - Parallel Compilation
    - tpd
    - Messages

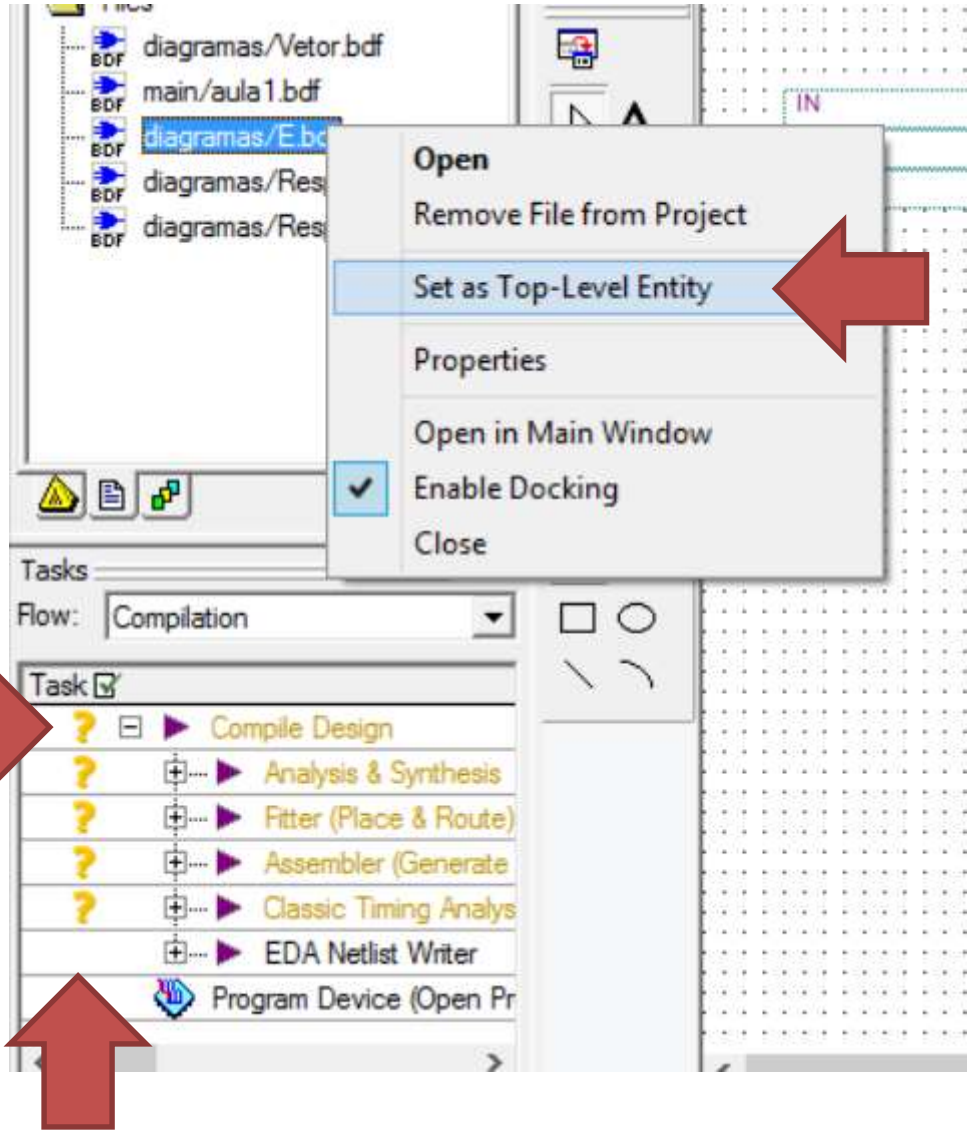
Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time	From	T	From Clock	To Clock	Failed Paths
1	Worst-case tpd	N/A	None	8.812 ns	A[0]			--	0
2	Total number of failed paths								0

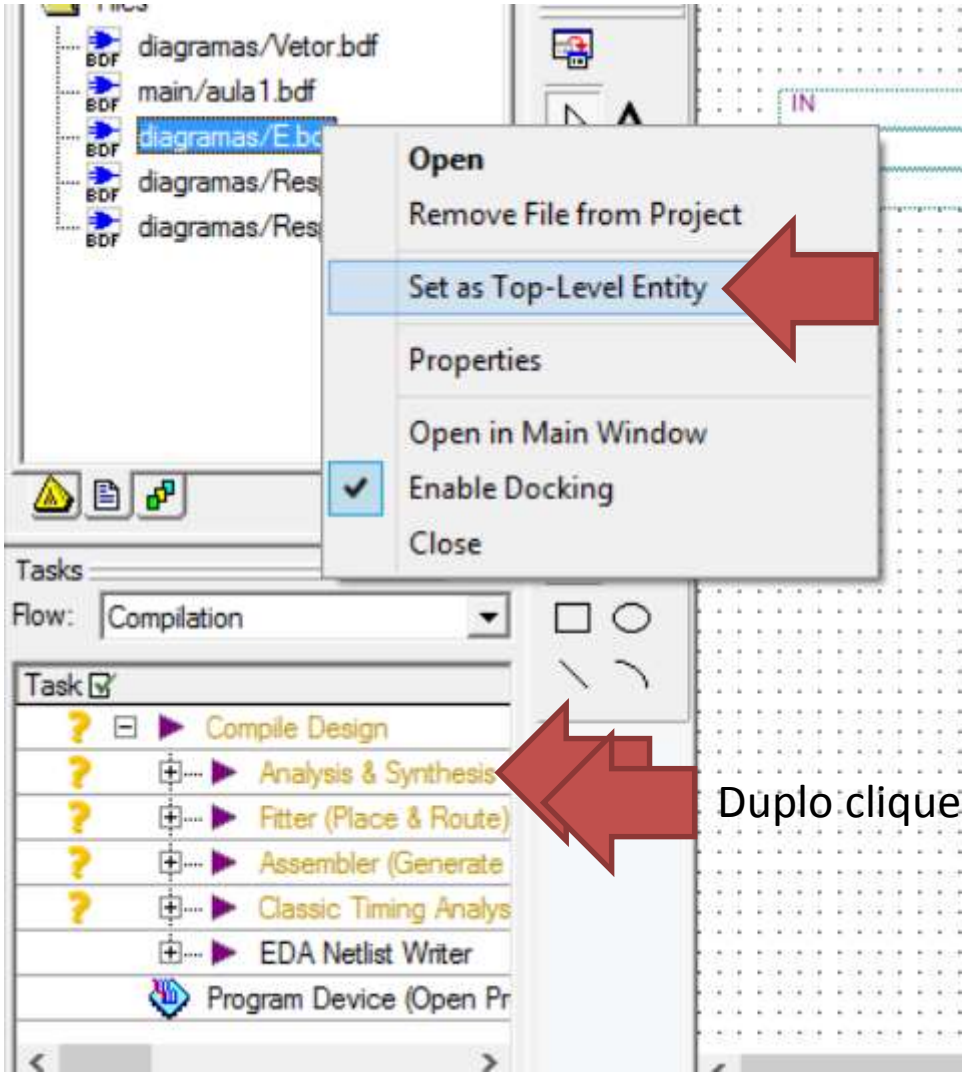

Type
Message
Critical Warning: No exact pin location assignment(s) for 6 pins of 6 total pins
Info: Pin Sinal not assigned to an exact location on the device
Info: Pin A[1] not assigned to an exact location on the device
Info: Pin A[2] not assigned to an exact location on the device
Info: Pin P[1] not assigned to an exact location on the device
Info: Pin P[0] not assigned to an exact location on the device
Info: Pin A[0] not assigned to an exact location on the device
System (3)
Processing (60)
Extra Info
Info (51)
Warning (8)
ning (1)
pressed (6)
Flag


Type
Message
Warning: Pin "P[1..0]" is missing source
Warning: Primitive "NOT" of instance "inst" not used
Warning: Primitive "NOT" of instance "inst1" not used
Warning: Output pins are stuck at VCC or GND
Warning: Design contains 2 input pin(s) that do not drive logic
Warning: Feature LogicLock is only available with a valid subscription license. Please purchase a software subscription to gain full access to this feature.
Warning: Found 3 output pins without output pin load capacitance assignment
Warning: The Reserve All Unused Pins setting has not been specified, and will default to 'As output driving ground'.

Altera aqui



Alterando Top level Aqui


diagramas/Vetor.bdf
main/aula1.bdf
diagramas/E.bd
diagramas/Res
diagramas/Res
Open
Remove File from Project
Set as Top-Level Entity
Properties
Open in Main Window
Enable Docking
Close
IN
Tasks
Flow:
Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate
Classic Timing Analys
EDA Netlist Writer
Program Device (Open Pr
Duplo clique

Block1.bdf

Compilation Report - Flow Summary

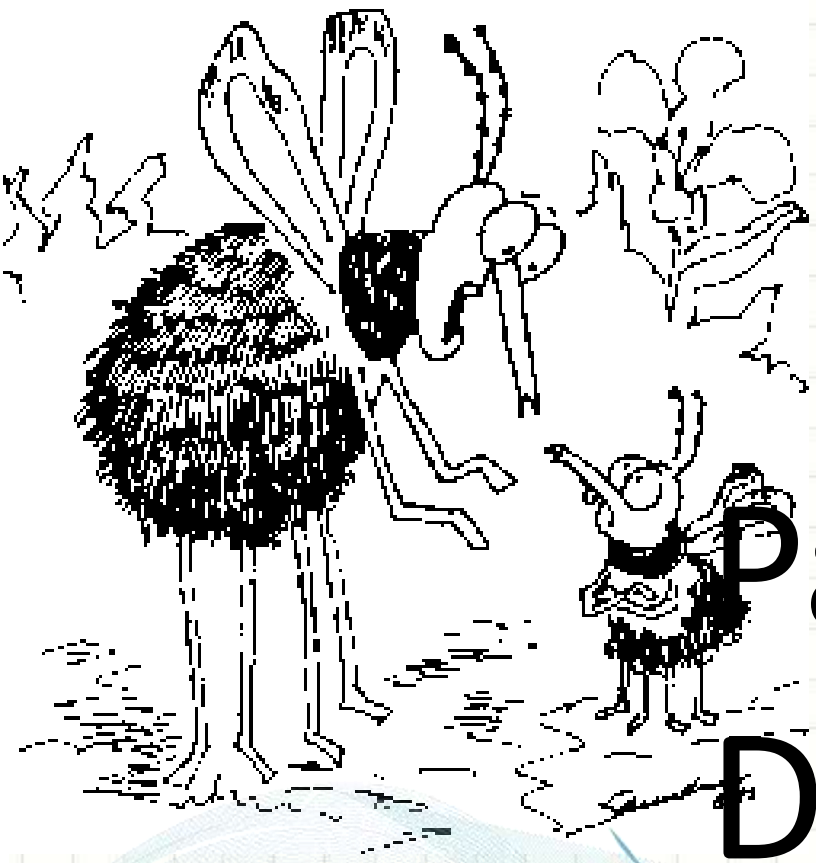
- Compilation Report
  - Legal Notice
  - Flow Summary
  - Flow Settings
  - Flow Non-Default Global Se
  - Flow Elapsed Time
  - Flow OS Summary
  - Flow Log
  - Analysis & Synthesis
  - Fitter
  - Assembler
  - Timing Analyzer

Flow Summary

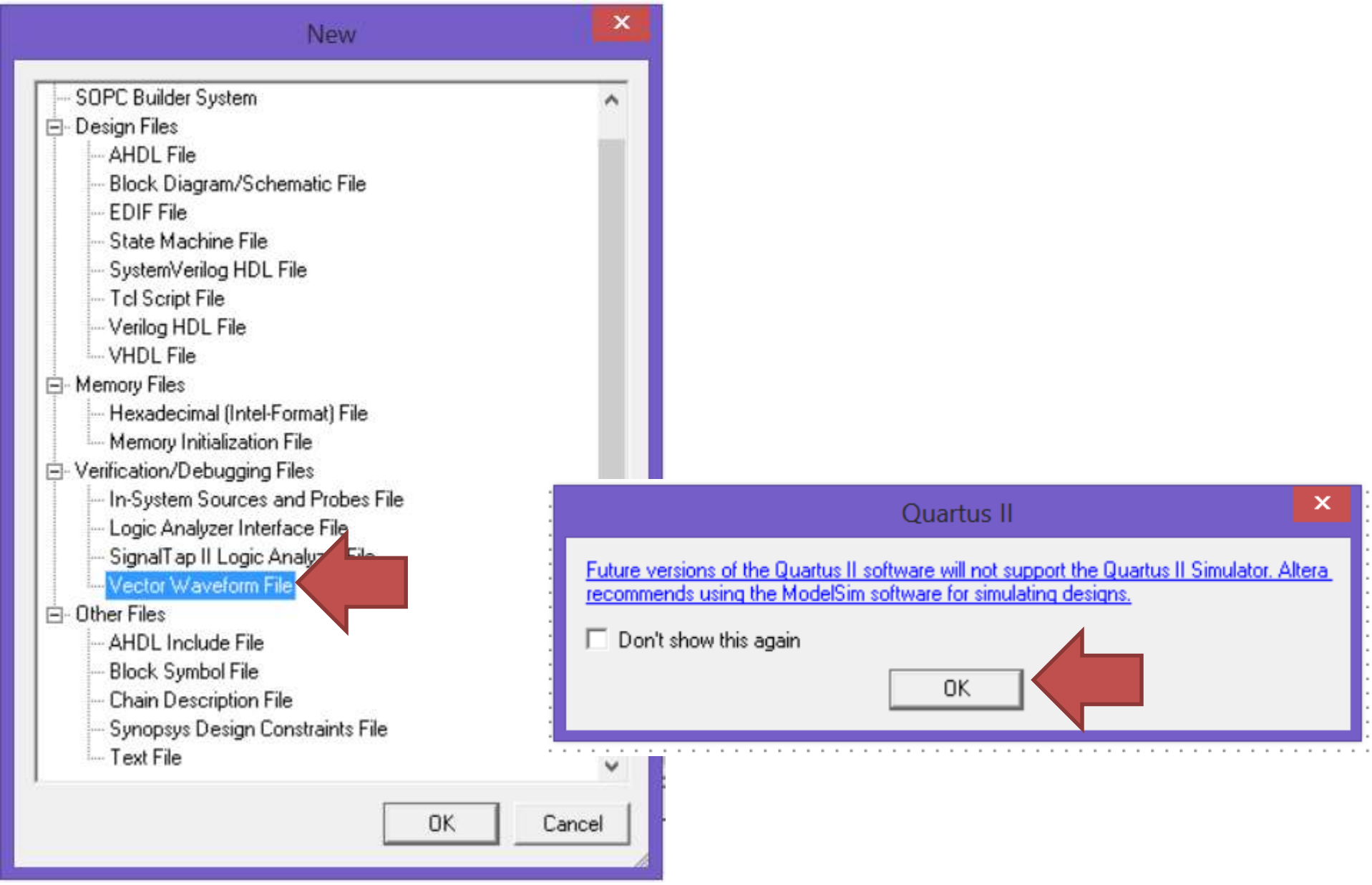
Flow Status	Successful - Tue Dec 03 00:08:53 2013
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	aula1
Top-level Entity Name	Vetor
Family	Cyclone II
Device	EP2C70F896C
Timing Models	Final
Met timing requirements	Yes
Total logic elements	0 / 68,416 (0 %)
Total combinational functions	0 / 68,416 (0 %)
Dedicated logic registers	0 / 68,416 (0 %)
Total registers	0
Total pins	6 / 622 (< 1 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

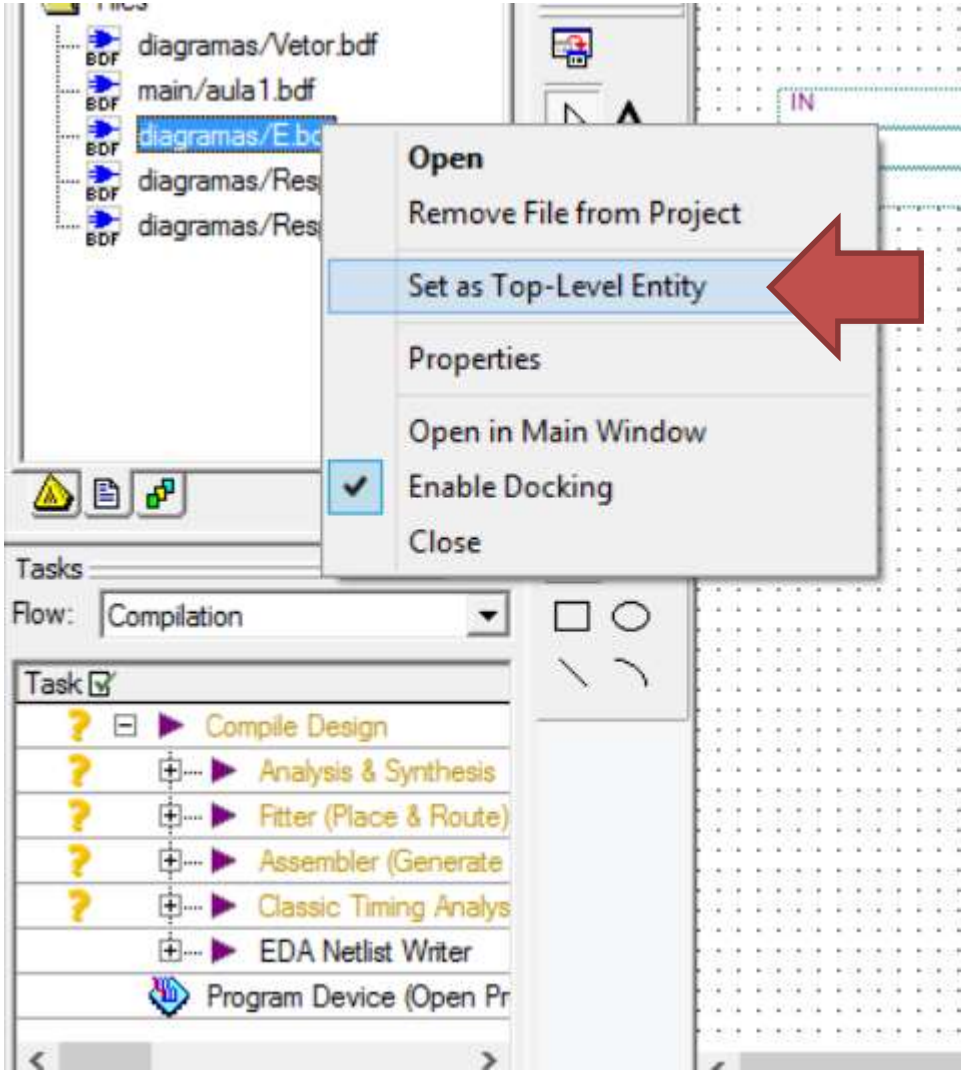
Exercício 2

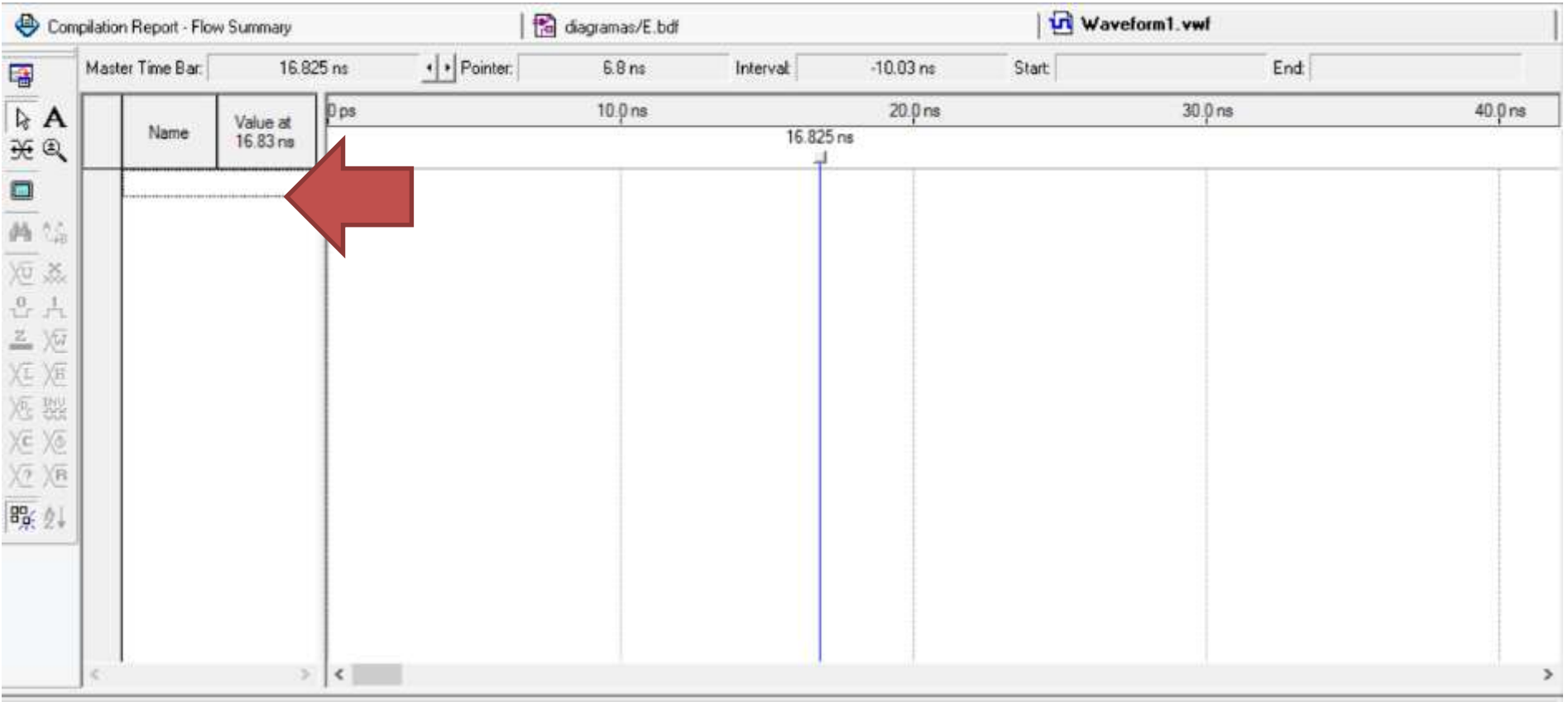
1. Construir por BDF
    1. (A ^ B) OR2 (NÃO Compilar)
2. Adicionar ao projeto:
    1. o vetor construido

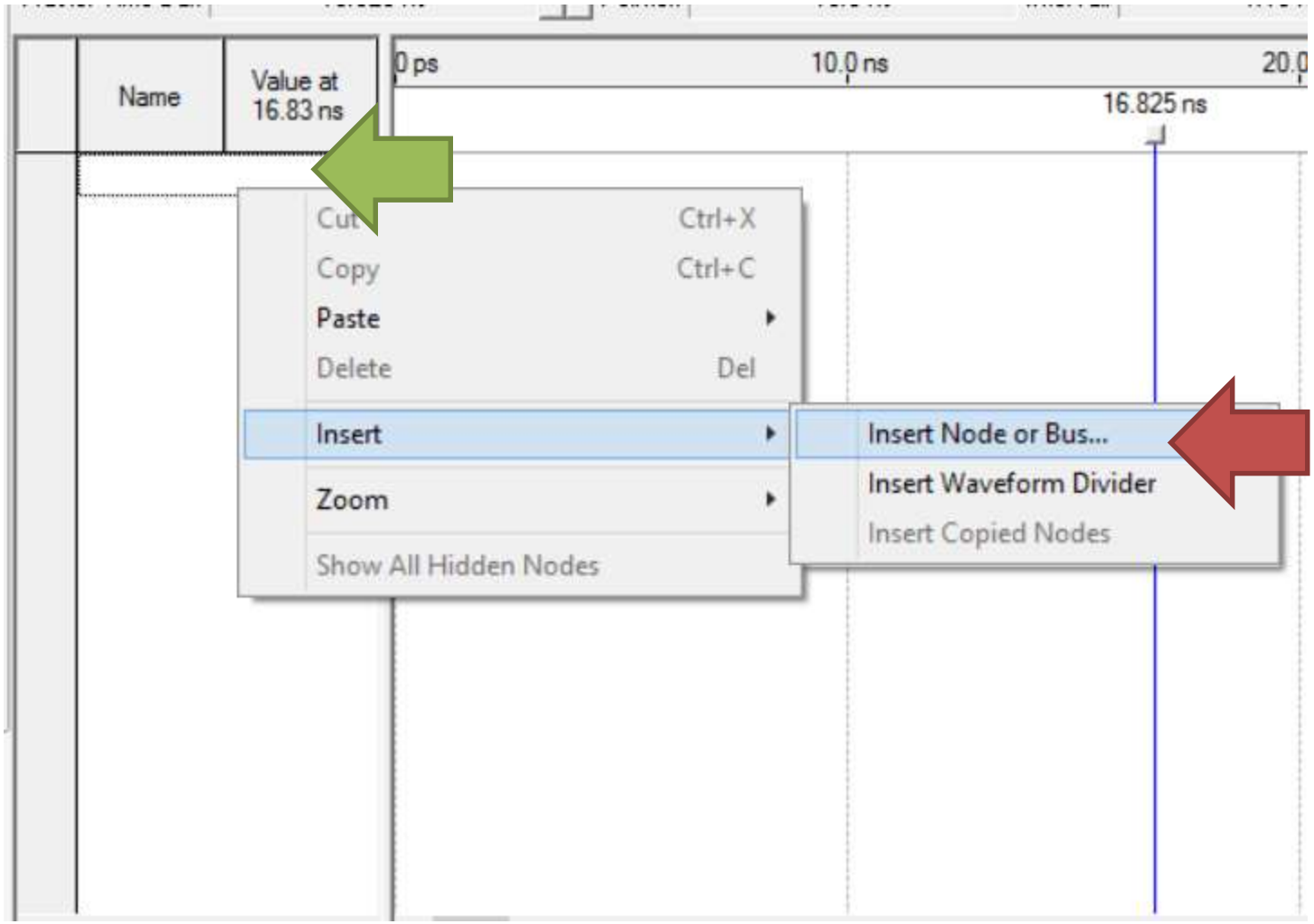


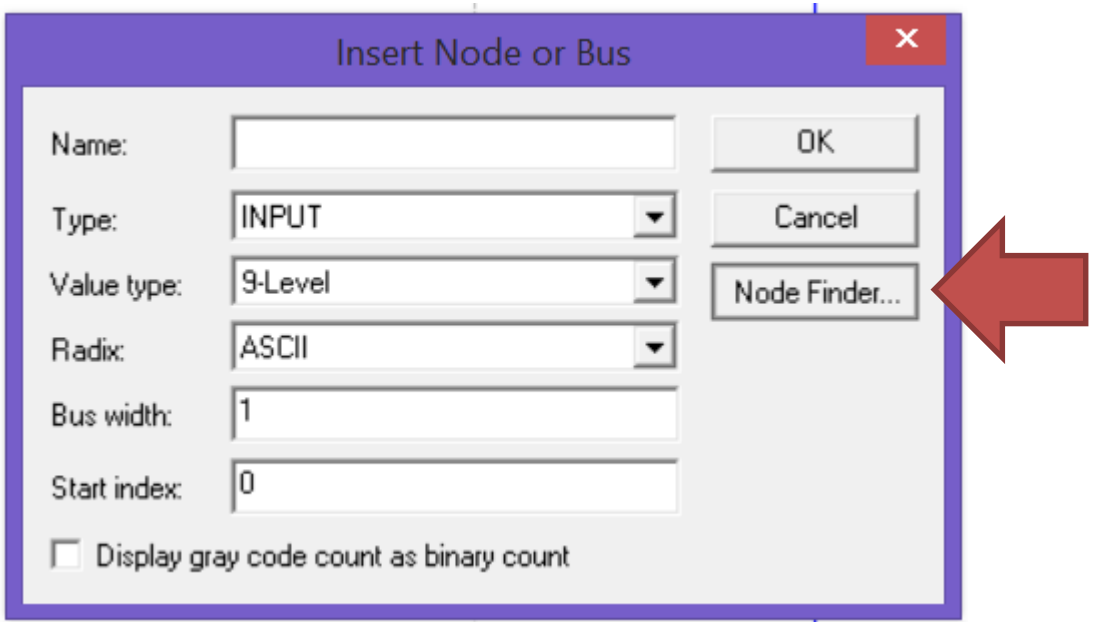
Parte 3: Debugando

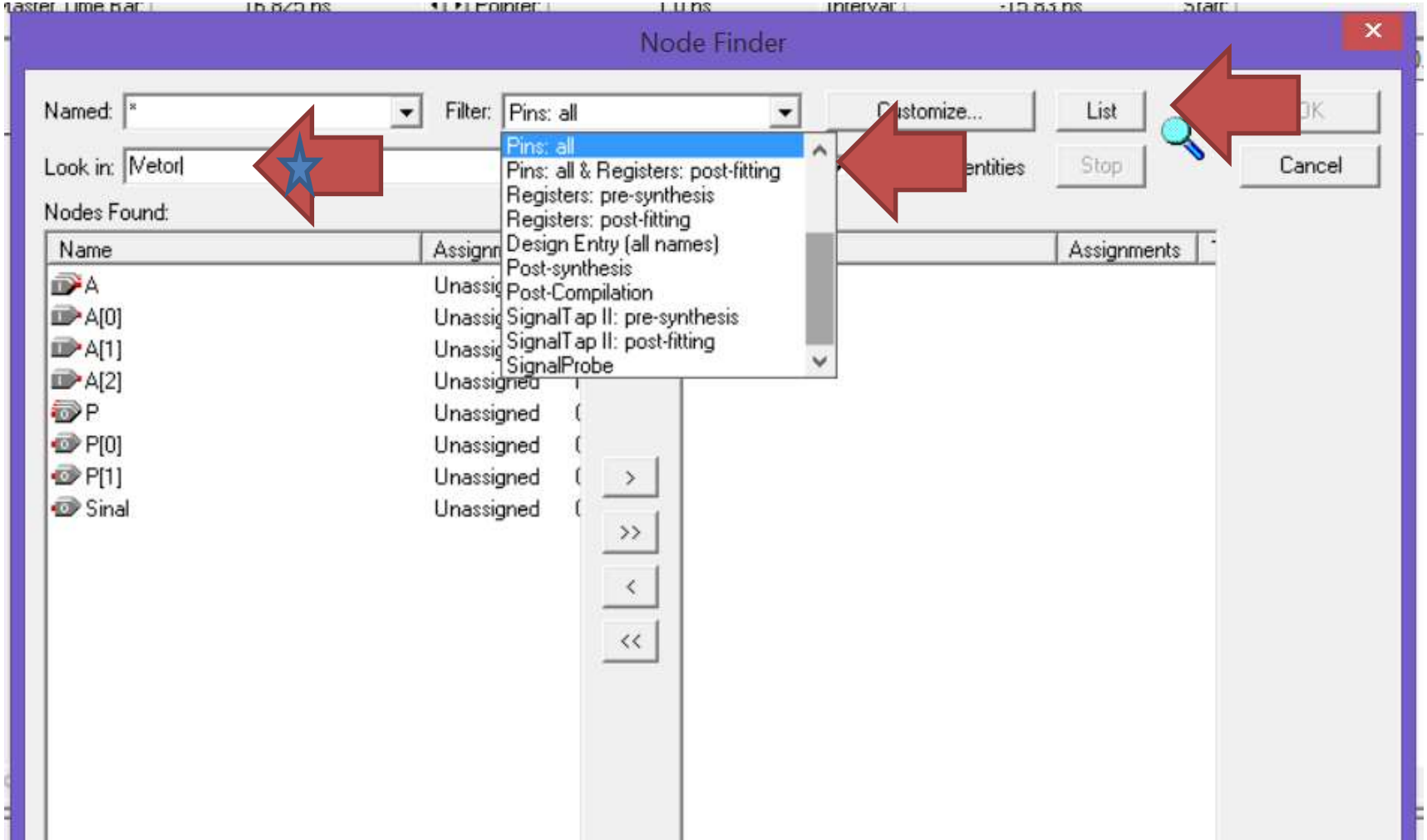

New
SOPC Builder System
Design Files
AHDL File
Block Diagram/Schematic File
EDIF File
State Machine File
SystemVerilog HDL File
Tcl Script File
Verilog HDL File
VHDL File
Memory Files
Hexadecimal (Intel-Format) File
Memory Initialization File
Verification/Debugging Files
In-System Sources and Probes File
Logic Analyzer Interface File
SignalTap II Logic Analy
Vector Waveform File
Other Files
AHDL Include File
Block Symbol File
Chain Description File
Synopsys Design Constraints File
Text File
OK
Cancel
Quartus II
Future versions of the Quartus II software will not support the Quartus II Simulator. Altera recommends using the ModelSim software for simulating designs.
Don't show this again
OK

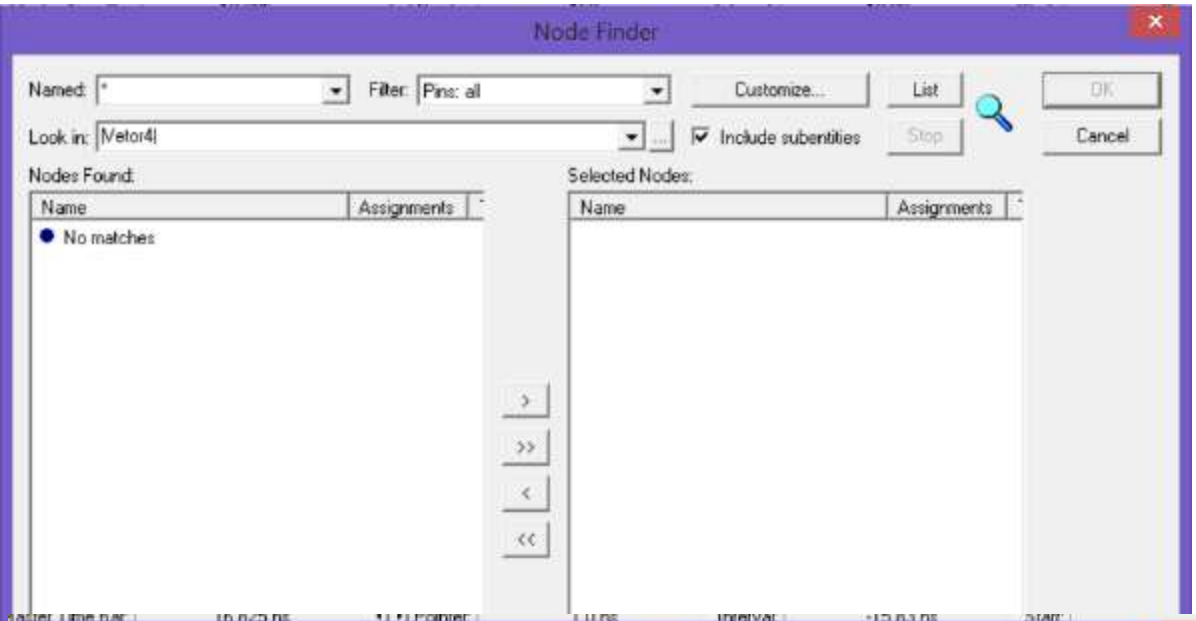

diagramas/Vetor.bdf
main/aula1.bdf
diagramas/E.bd
diagramas/Res
diagramas/Res
Open
Remove File from Project
Set as Top-Level Entity
Properties
Open in Main Window
Enable Docking
Close
IN
Tasks
Flow:
Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate
Classic Timing Analys
EDA Netlist Writer
Program Device (Open Pr


Compilation Report - Flow Summary
diagramas/E.bdf
Waveform1.vwf
Master Time Bar:
16.825 ns
Pointer:
6.8 ns
Interval:
-10.03 ns
Start:
End:
Name
Value at
16.83 ns
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
16.825 ns


Name
Value at
16.83 ns
0 ps
10.0 ns
20.0
16.825 ns
Cut
Ctrl+X
Copy
Ctrl+C
Paste
Delete
Del
Insert
Zoom
Show All Hidden Nodes
Insert Node or Bus...
Insert Waveform Divider
Insert Copied Nodes

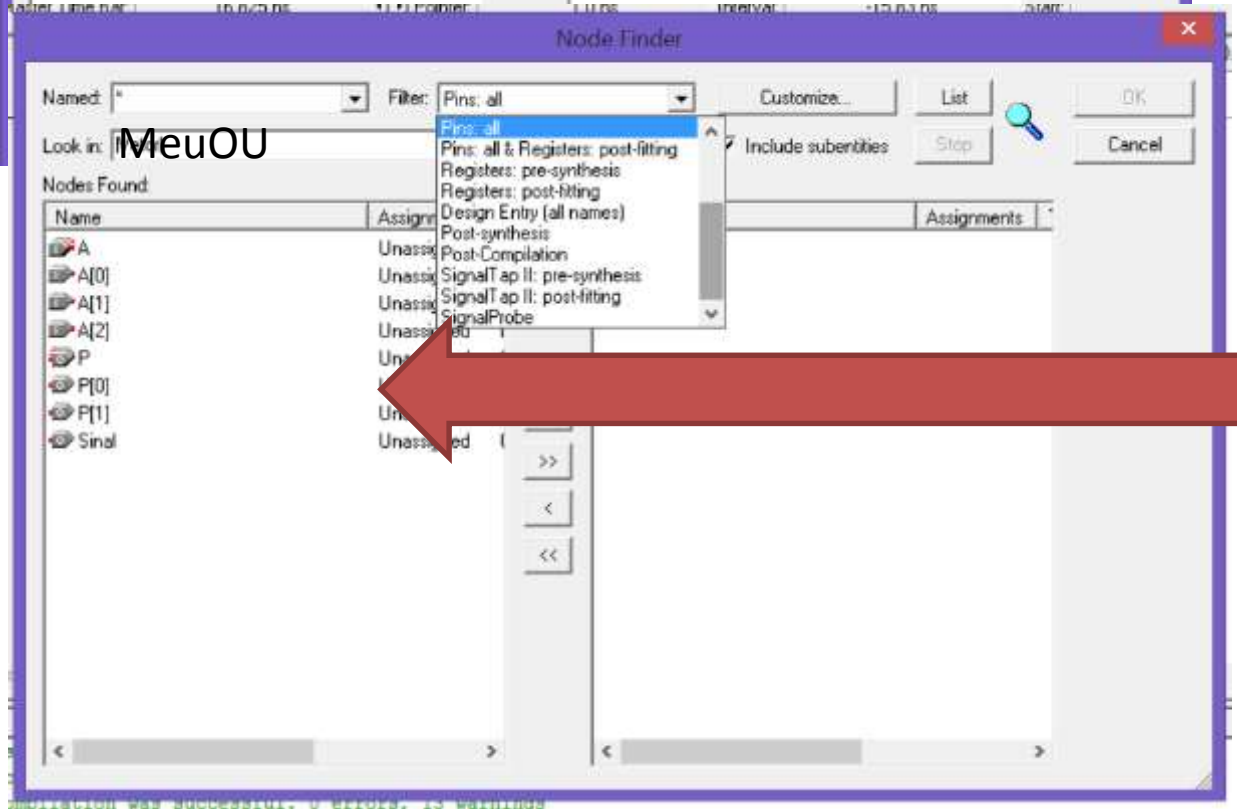

Insert Node or Bus
Name:
Type:
INPUT
Value type:
9-Level
Radix:
ASCII
Bus width:
1
Start index:
0
Display gray code count as binary count
OK
Cancel
Node Finder...


Node Finder
Named:
*
Filter:
Pins: all
Customize...
List
OK
Look in:
|Vetor|
Stop
Cancel
Nodes Found:
Pins: all
Pins: all & Registers: post-fitting
Registers: pre-synthesis
Registers: post-fitting
Design Entry (all names)
Post-synthesis
Post-Compilation
SignalTap II: pre-synthesis
SignalTap II: post-fitting
SignalProbe
Name
Assignments
A
A[0]
A[1]
A[2]
P
P[0]
P[1]
Sinal
Unassigned
>
>>
<
<<



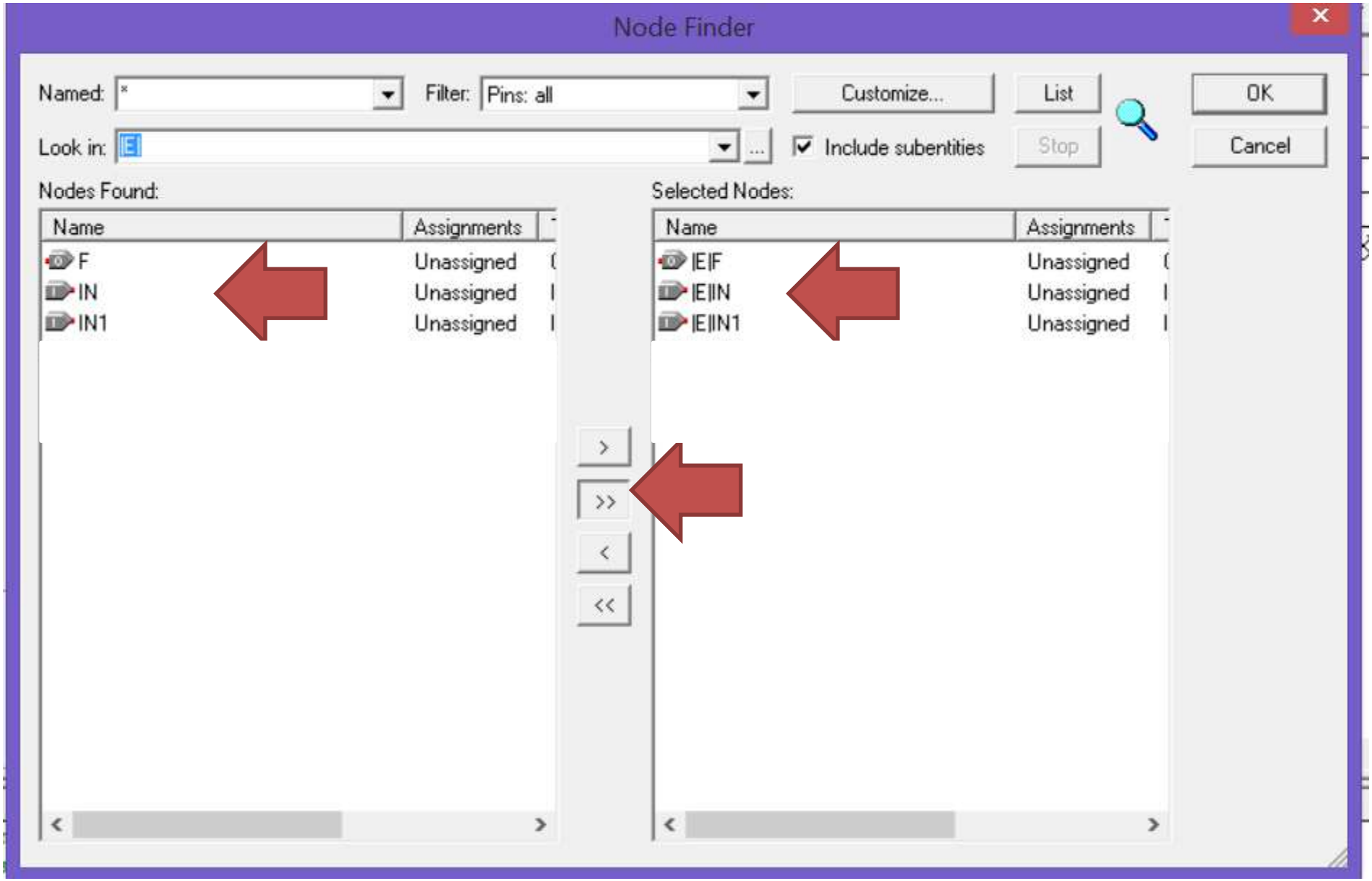
Set Top Level

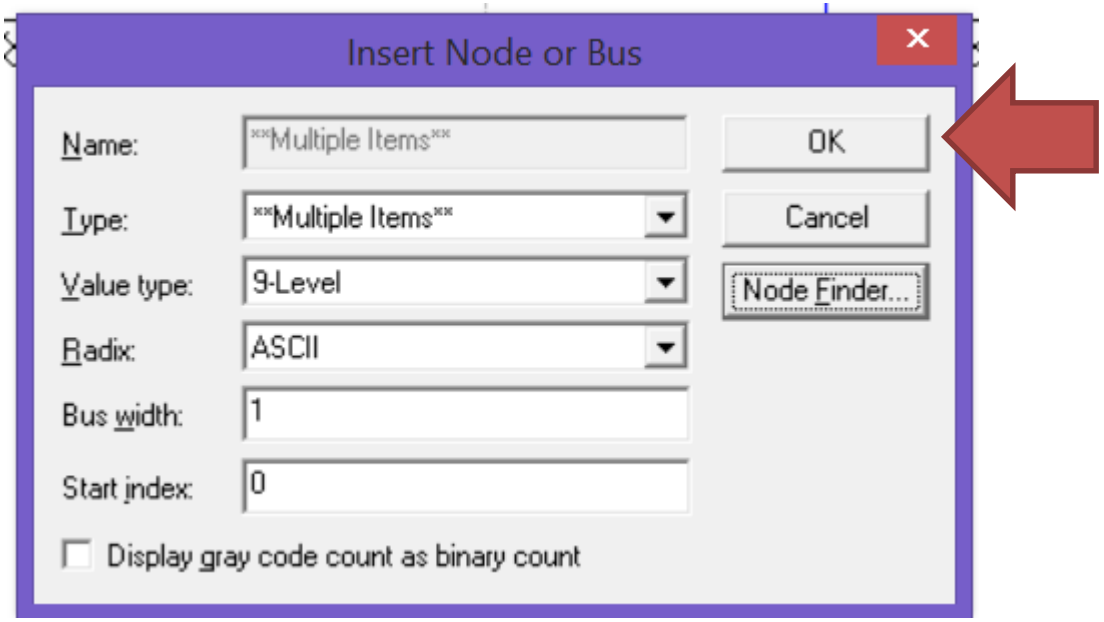
Problemas!!



MeuOU

Não Compilado


Node Finder
Named: *
Filter: Pins: all
Customize...
List
OK
Look in: E
Include subentities
Stop
Cancel
Nodes Found:
Name
Assignments
F
Unassigned
IN
Unassigned
IN1
Unassigned
Selected Nodes:
Name
Assignments
E|F
Unassigned
E|IN
Unassigned
E|IN1
Unassigned
>
>>
<
<<


Insert Node or Bus
Name:
Multiple Items
Type:
Multiple Items
Value type:
9-Level
Radix:
ASCII
Bus width:
1
Start index:
0
Display gray code count as binary count
OK
Cancel
Node Finder...

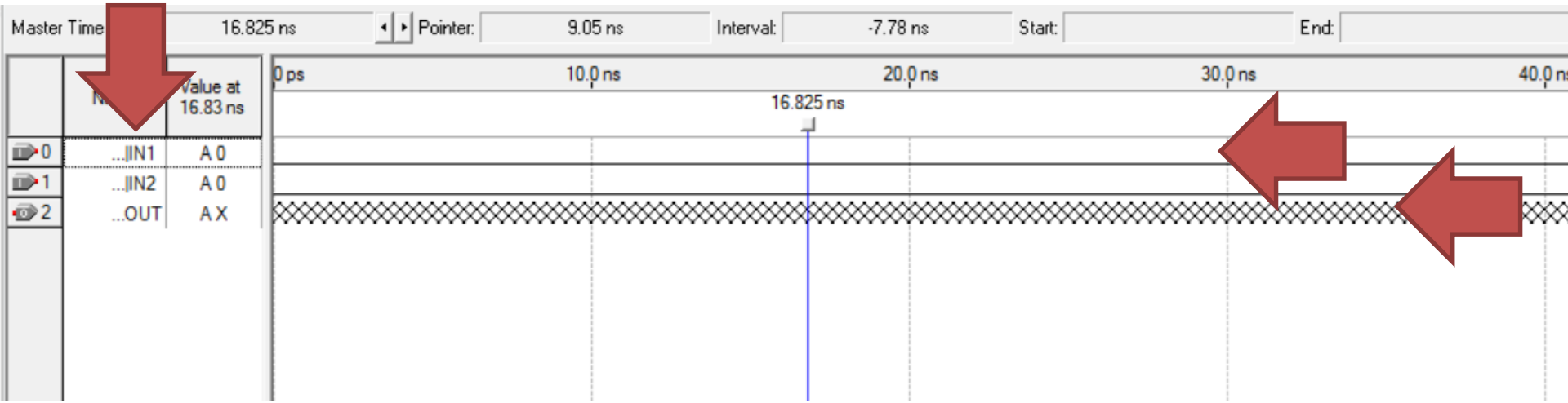

Master Time
16.825 ns
Pointer:
9.05 ns
Interval:
-7.78 ns
Start:
End:
Value at
16.83 ns
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
16.825 ns
0
...IN1
A 0
1
...IN2
A 0
2
...OUT
A X

Tabela verdade vs. Frequência

A	B	C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

2^2 ts

2^1 ts

2^0 t

Block1.bdf

Compilation Report - Flow Summary

- Compilation Report
  - Legal Notice
  - Flow Summary
  - Flow Settings
  - Flow Non-Default Global Se
  - Flow Elapsed Time
  - Flow OS Summary
  - Flow Log
  - Analysis & Synthesis
  - Fitter
  - Assembler
  - Timing Analyzer

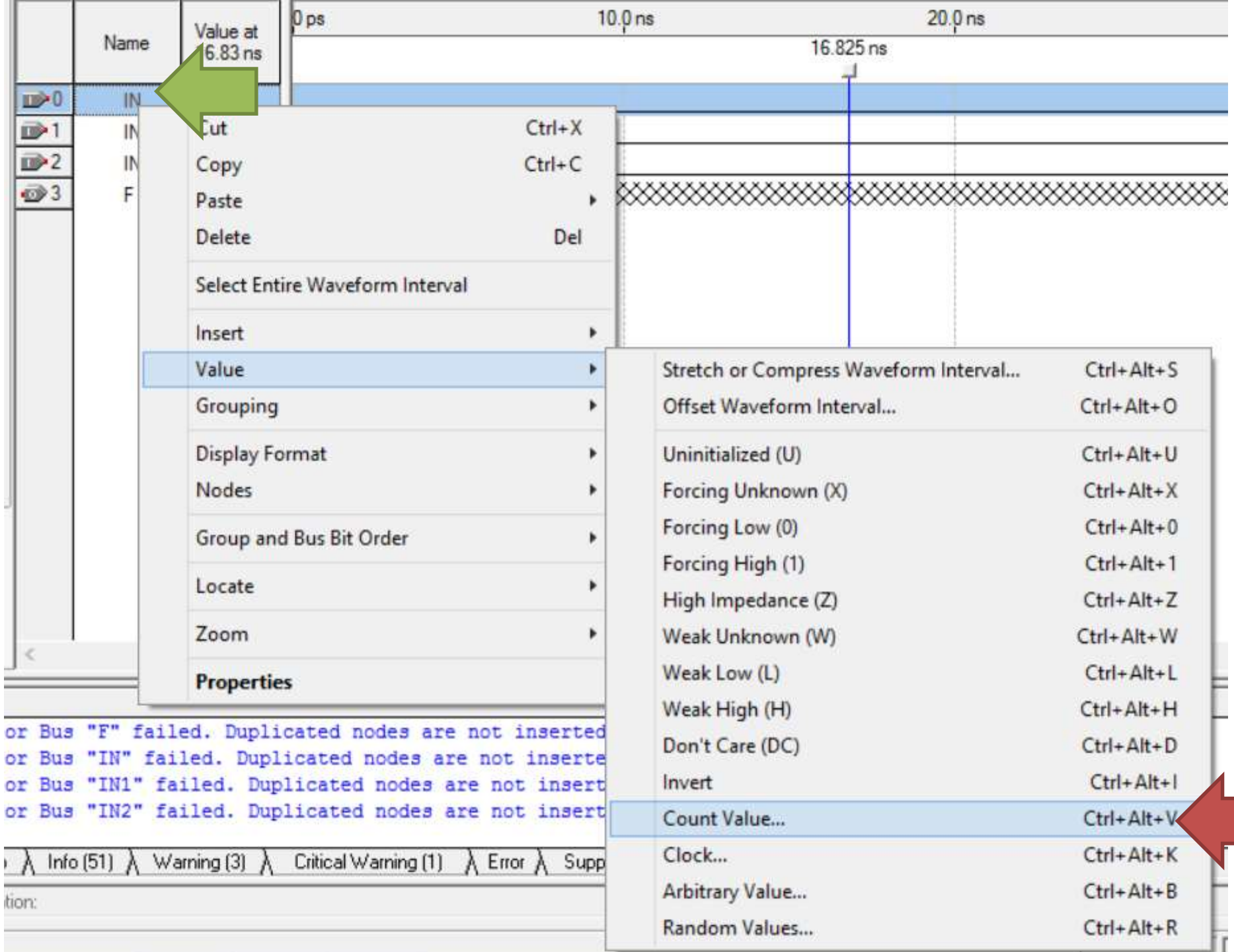
Flow Summary

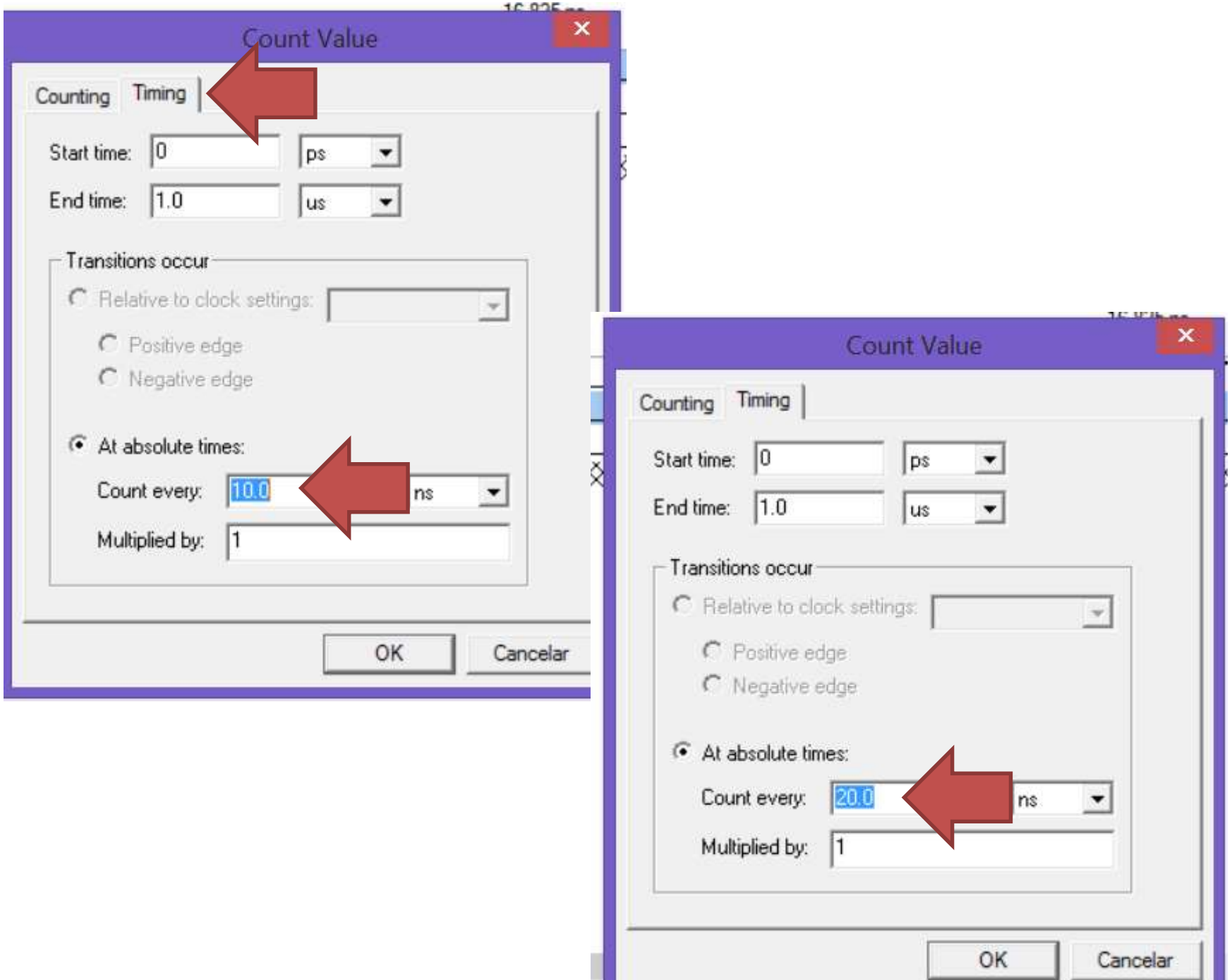
Flow Status	Successful - Tue Dec 03 00:08:53 2013
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	aula1
Top-level Entity Name	Vetor
Family	Cyclone II
Device	EP2C70F896C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	0 / 68,416 (0 %)
Total combinational functions	0 / 68,416 (0 %)
Dedicated logic registers	0 / 68,416 (0 %)
Total registers	0
Total pins	6 / 622 (< 1 %)

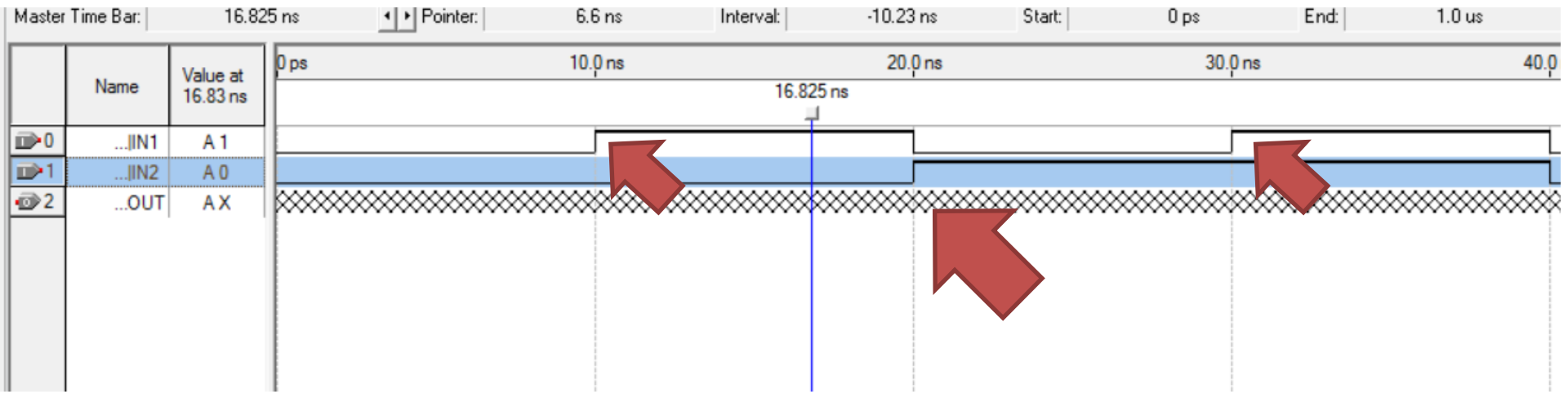
- Compilation Report
  - Legal Notice
  - Flow Summary
  - Flow Settings
  - Flow Non-Default Global Se
  - Flow Elapsed Time
  - Flow OS Summary
  - Flow Log
  - Analysis & Synthesis
  - Fitter
  - Assembler
  - Timing Analyzer
    - Summary
    - Settings
    - Parallel Compilation
    - tpd
    - Messages

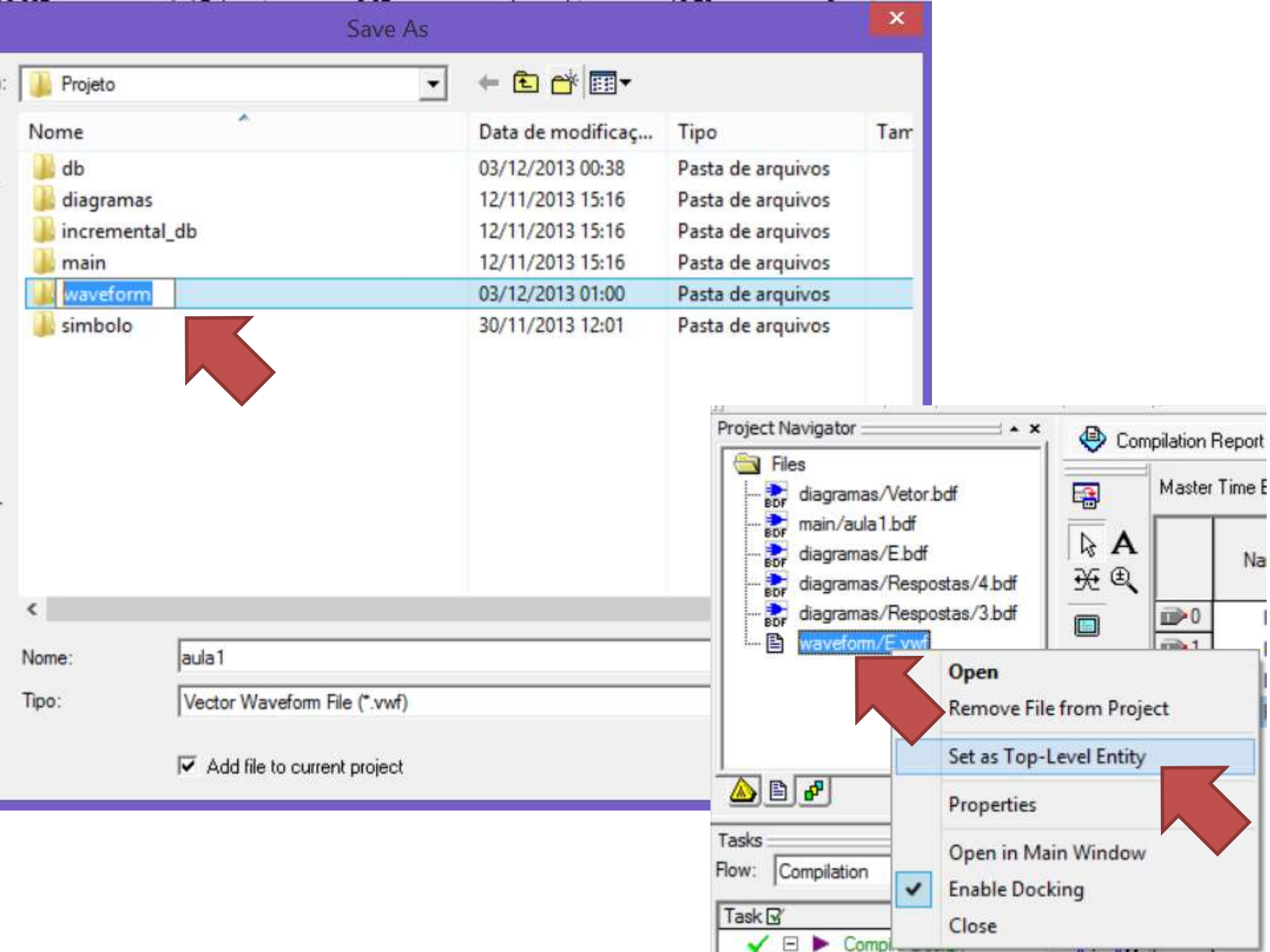
Timing Analyzer Summary

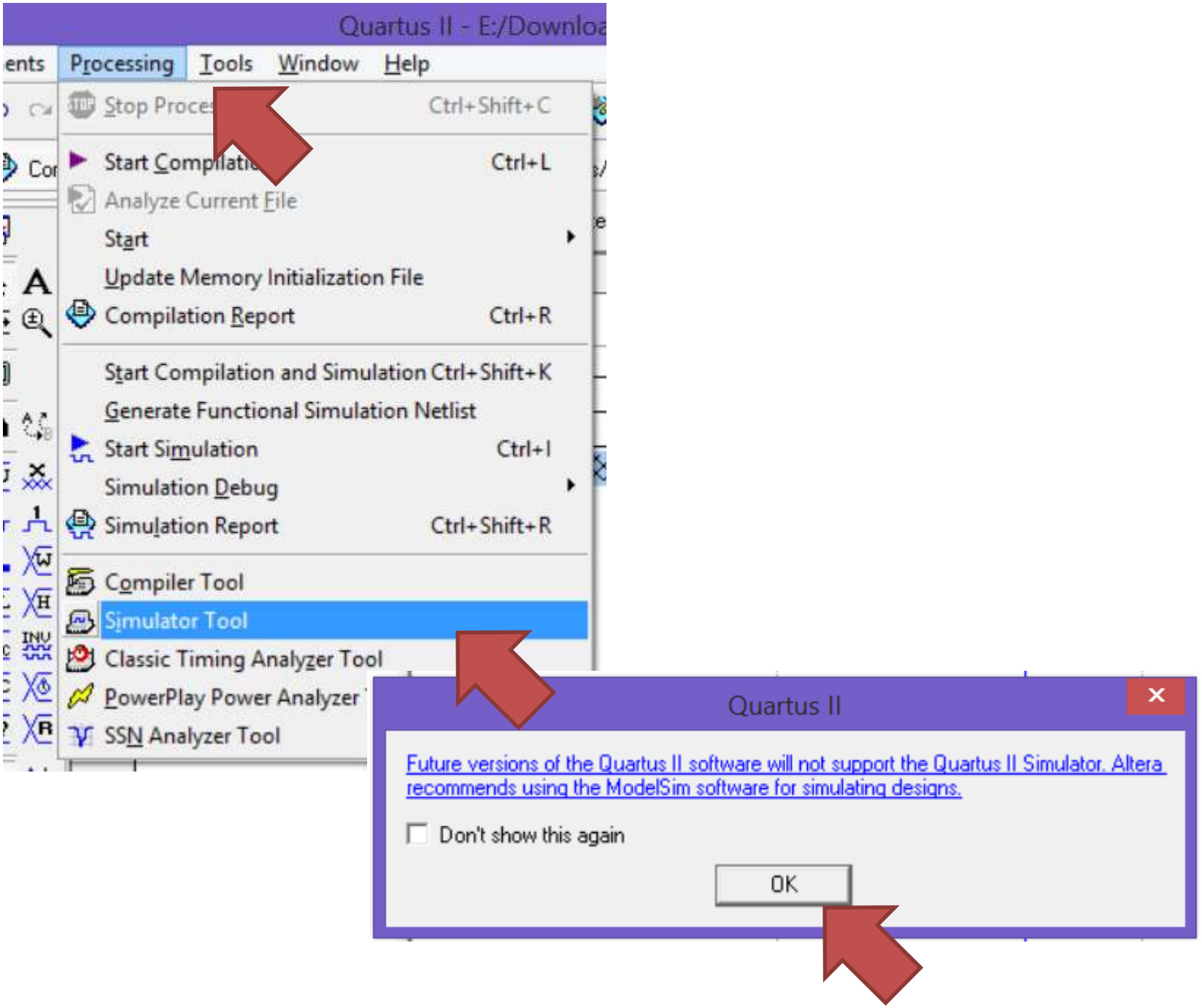
	Type	Slack	Required Time	Actual Time	From	To	From Clock	To Clock	Failed Paths
1	Worst-case tpd	N/A	None	8.812 ns				--	0
2	Total number of failed paths								0

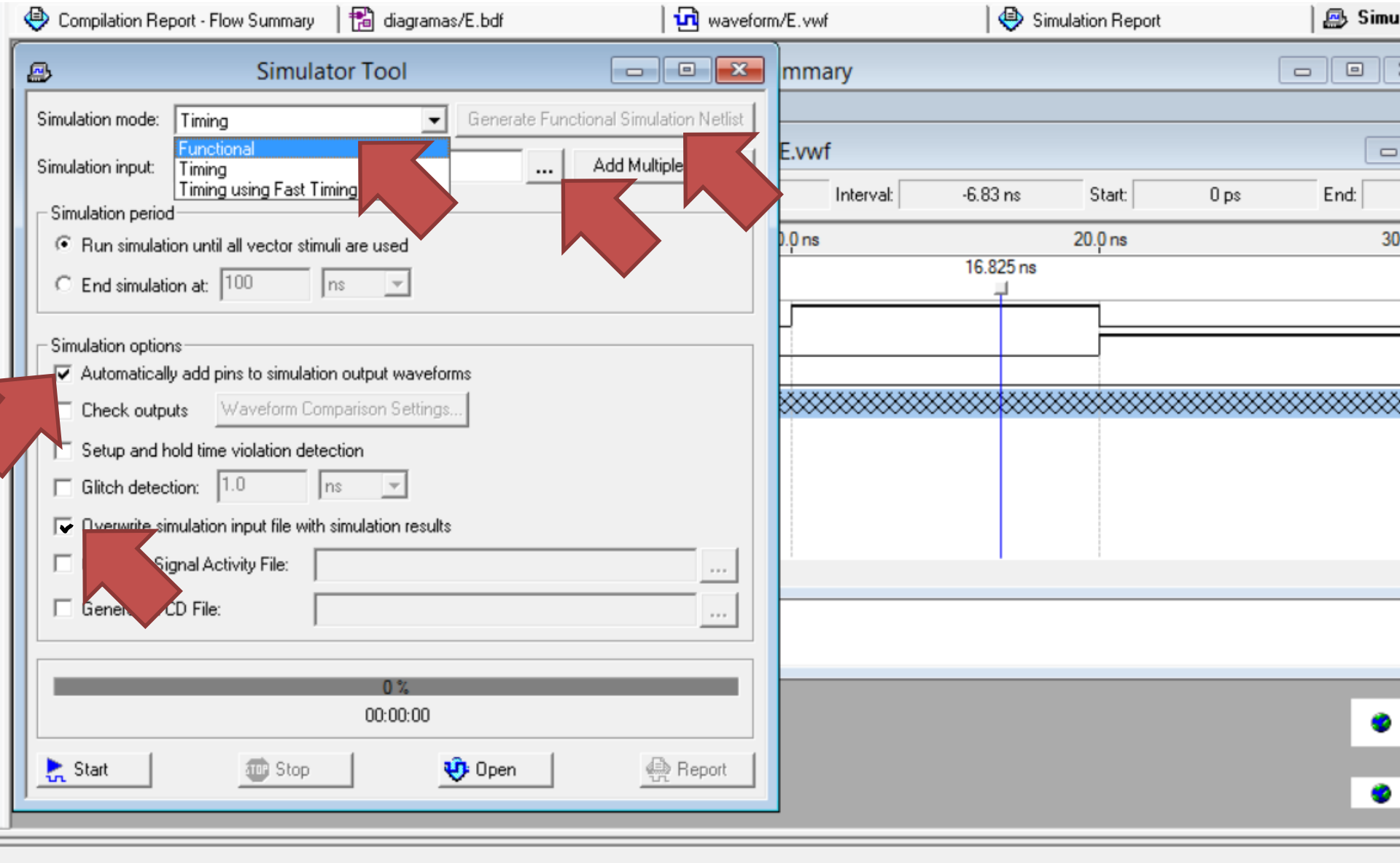

Name
Value at 6.83 ns
0 ps
10.0 ns
20.0 ns
16.825 ns
0
1
2
3
IN
IN
IN
F
Cut Ctrl+X
Copy Ctrl+C
Paste
Delete Del
Select Entire Waveform Interval
Insert
Value
Grouping
Display Format
Nodes
Group and Bus Bit Order
Locate
Zoom
Properties
Stretch or Compress Waveform Interval... Ctrl+Alt+S
Offset Waveform Interval... Ctrl+Alt+O
Uninitialized (U) Ctrl+Alt+U
Forcing Unknown (X) Ctrl+Alt+X
Forcing Low (0) Ctrl+Alt+0
Forcing High (1) Ctrl+Alt+1
High Impedance (Z) Ctrl+Alt+Z
Weak Unknown (W) Ctrl+Alt+W
Weak Low (L) Ctrl+Alt+L
Weak High (H) Ctrl+Alt+H
Don't Care (DC) Ctrl+Alt+D
Invert Ctrl+Alt+I
Count Value... Ctrl+Alt+V
Clock... Ctrl+Alt+K
Arbitrary Value... Ctrl+Alt+B
Random Values... Ctrl+Alt+R
or Bus "F" failed. Duplicated nodes are not inserted
or Bus "IN" failed. Duplicated nodes are not inserte
or Bus "IN1" failed. Duplicated nodes are not insert
or Bus "IN2" failed. Duplicated nodes are not insert
Info (51)
Warning (3)
Critical Warning (1)
Error
Supp

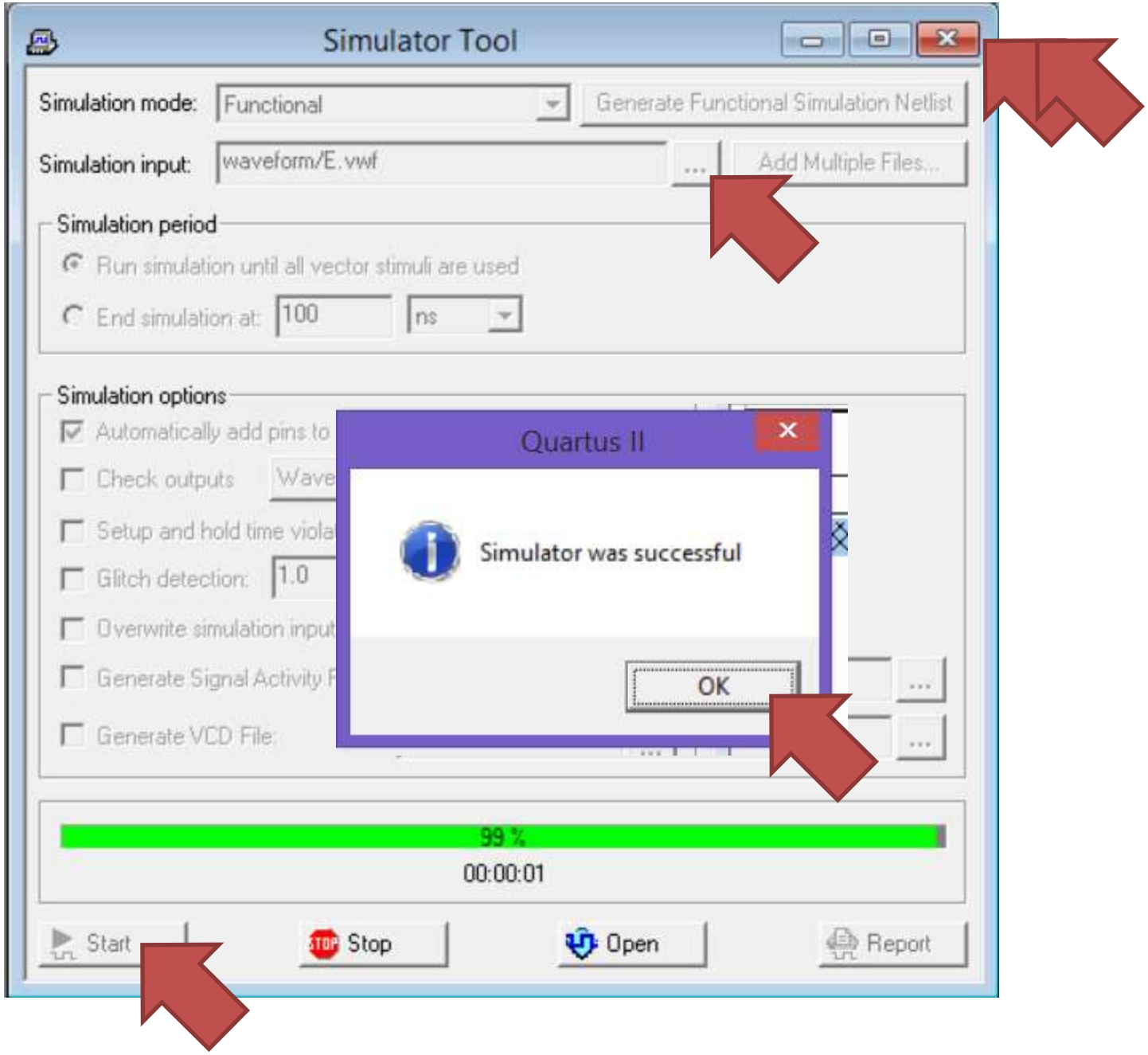

Count Value
Counting
Timing
Start time:
0
ps
End time:
1.0
us
Transitions occur
Relative to clock settings:
Positive edge
Negative edge
At absolute times:
Count every:
10.0
ns
Multiplied by:
1
OK
Cancelar
Count Value
Counting
Timing
Start time:
0
ps
End time:
1.0
us
Transitions occur
Relative to clock settings:
Positive edge
Negative edge
At absolute times:
Count every:
20.0
ns
Multiplied by:
1
OK
Cancelar

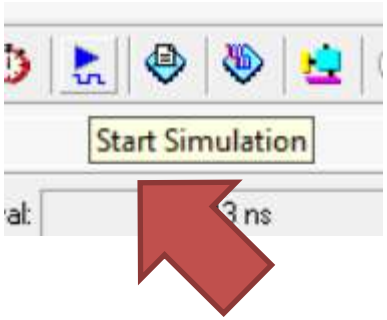

Master Time Bar: 16.825 ns
Pointer: 6.6 ns
Interval: -10.23 ns
Start: 0 ps
End: 1.0 us
Name
Value at 16.83 ns
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0
16.825 ns
0 ...IIN1 A 1
1 ...IIN2 A 0
2 ...OUT A X

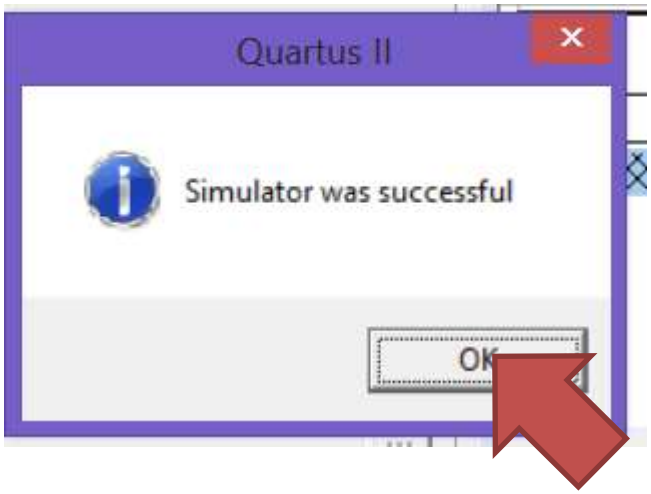

Save As
Projeto
Nome
Data de modificaç...
Tipo
Tam
db
03/12/2013 00:38
Pasta de arquivos
diagramas
12/11/2013 15:16
Pasta de arquivos
incremental_db
12/11/2013 15:16
Pasta de arquivos
main
12/11/2013 15:16
Pasta de arquivos
waveform
03/12/2013 01:00
Pasta de arquivos
simbolo
30/11/2013 12:01
Pasta de arquivos
Nome:
aula1
Tipo:
Vector Waveform File (*.vwf)
Add file to current project
Project Navigator
Files
diagramas/Vetor.bdf
main/aula1.bdf
diagramas/E.bdf
diagramas/Respostas/4.bdf
diagramas/Respostas/3.bdf
waveform/E.vwf
Compilation Report
Master Time
Open
Remove File from Project
Set as Top-Level Entity
Properties
Open in Main Window
Enable Docking
Close
Tasks
Flow:
Compilation
Task

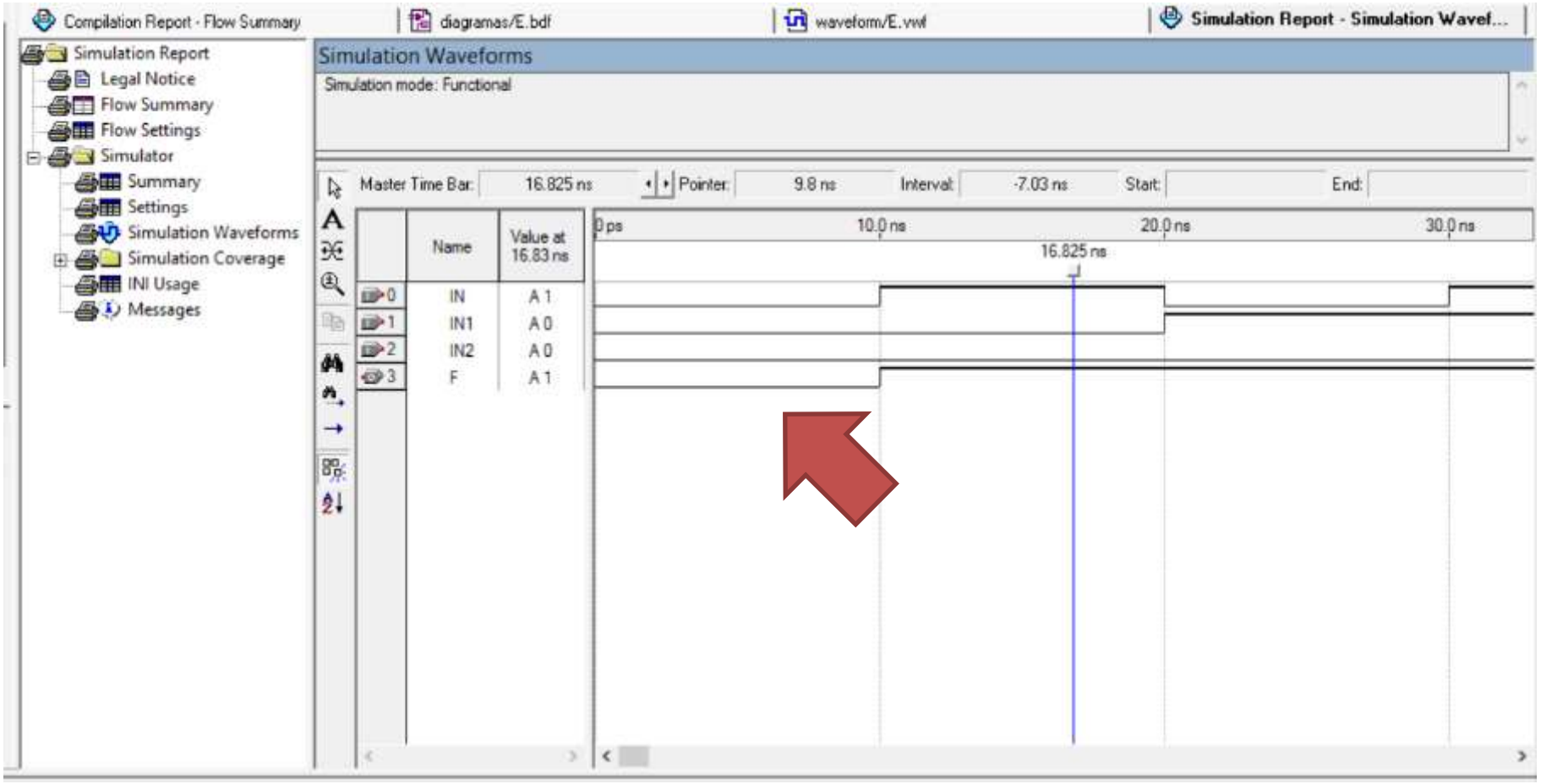

Quartus II - E:/Downloa
ents
Processing
Tools
Window
Help
Stop Proces
Ctrl+Shift+C
Start Compilati
Ctrl+L
Analyze Current File
Start
Update Memory Initialization File
Compilation Report
Ctrl+R
Start Compilation and Simulation
Ctrl+Shift+K
Generate Functional Simulation Netlist
Start Simulation
Ctrl+I
Simulation Debug
Simulation Report
Ctrl+Shift+R
Compiler Tool
Simulator Tool
Classic Timing Analyzer Tool
PowerPlay Power Analyzer
SSN Analyzer Tool
Quartus II
Future versions of the Quartus II software will not support the Quartus II Simulator. Altera recommends using the ModelSim software for simulating designs.
Don't show this again
OK


Compilation Report - Flow Summary
diagramas/E.bdf
waveform/E.vwf
Simulation Report
Simulator Tool
Simulation mode:
Timing
Functional
Timing
Timing using Fast Timing
Generate Functional Simulation Netlist
Simulation input:
Add Multiple
Simulation period
Run simulation until all vector stimuli are used
End simulation at:
100
ns
Simulation options
Automatically add pins to simulation output waveforms
Check outputs
Waveform Comparison Settings...
Setup and hold time violation detection
Glitch detection:
1.0
ns
Overwrite simulation input file with simulation results
Signal Activity File:
CD File:
0 %
00:00:00
Start
Stop
Open
Report
mmary
E.vwf
Interval:
-6.83 ns
Start:
0 ps
End:
20.0 ns
16.825 ns


Simulator Tool
Simulation mode:
Functional
Generate Functional Simulation Netlist
Simulation input:
waveform/E.vwf
...
Add Multiple Files...
Simulation period
Run simulation until all vector stimuli are used
End simulation at:
100
ns
Simulation options
Automatically add pins to
Check outputs
Wave
Setup and hold time viola
Glitch detection:
1.0
Overwrite simulation input
Generate Signal Activity
Generate VCD File:
Quartus II
Simulator was successful
OK
99 %
00:00:01
Start
Stop
Open
Report


Start Simulation

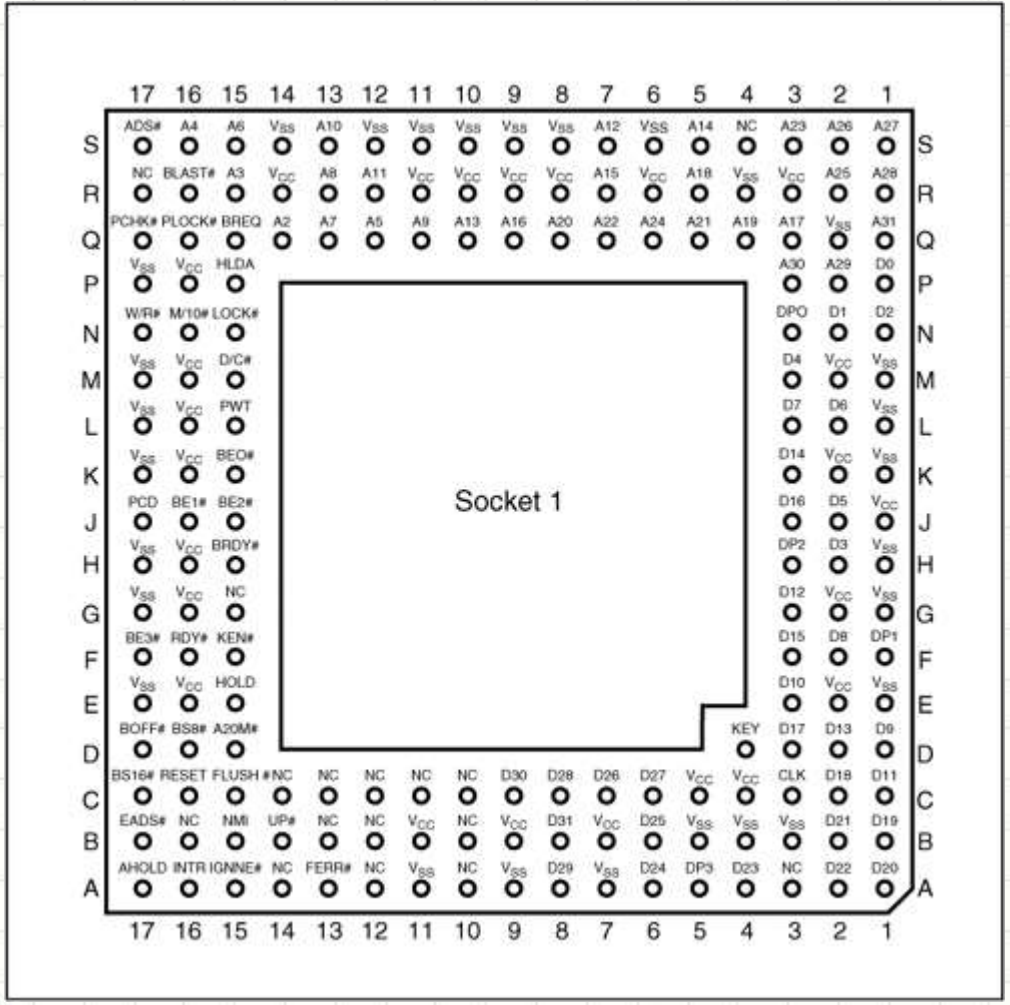

Quartus II
Simulator was successful
OK


Compilation Report - Flow Summary
diagramas/E.bdf
waveform/E.vwf
Simulation Report - Simulation Wavef...
Simulation Report
Legal Notice
Flow Summary
Flow Settings
Simulator
Summary
Settings
Simulation Waveforms
Simulation Coverage
INI Usage
Messages
Simulation Waveforms
Simulation mode: Functional
Master Time Bar: 16.825 ns
Pointer: 9.8 ns
Interval: -7.03 ns
Start:
End:
Name
Value at 16.83 ns
0 IN A 1
1 IN1 A 0
2 IN2 A 0
3 F A 1
0 ps
10.0 ns
20.0 ns
30.0 ns
16.825 ns

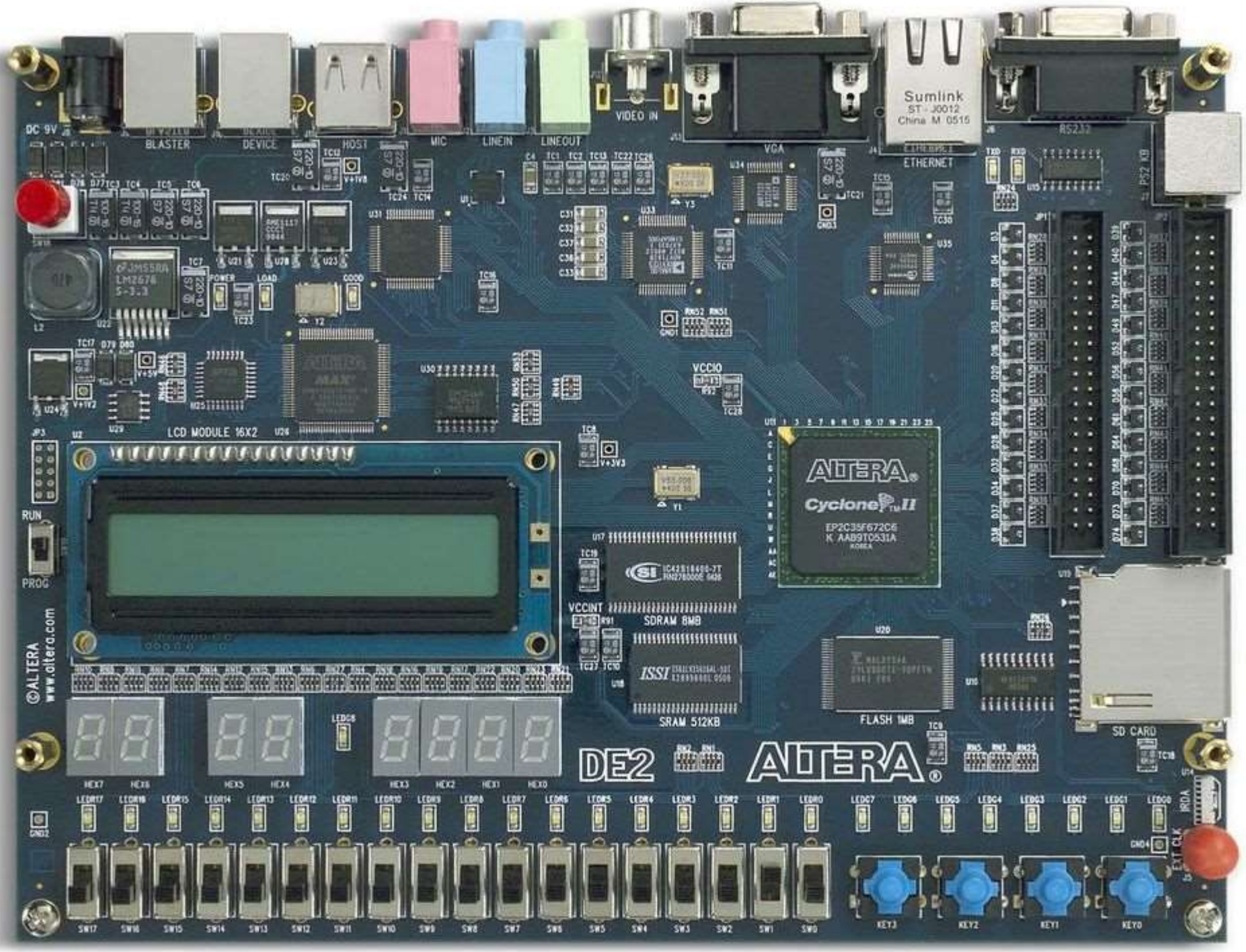
Exercício 3:

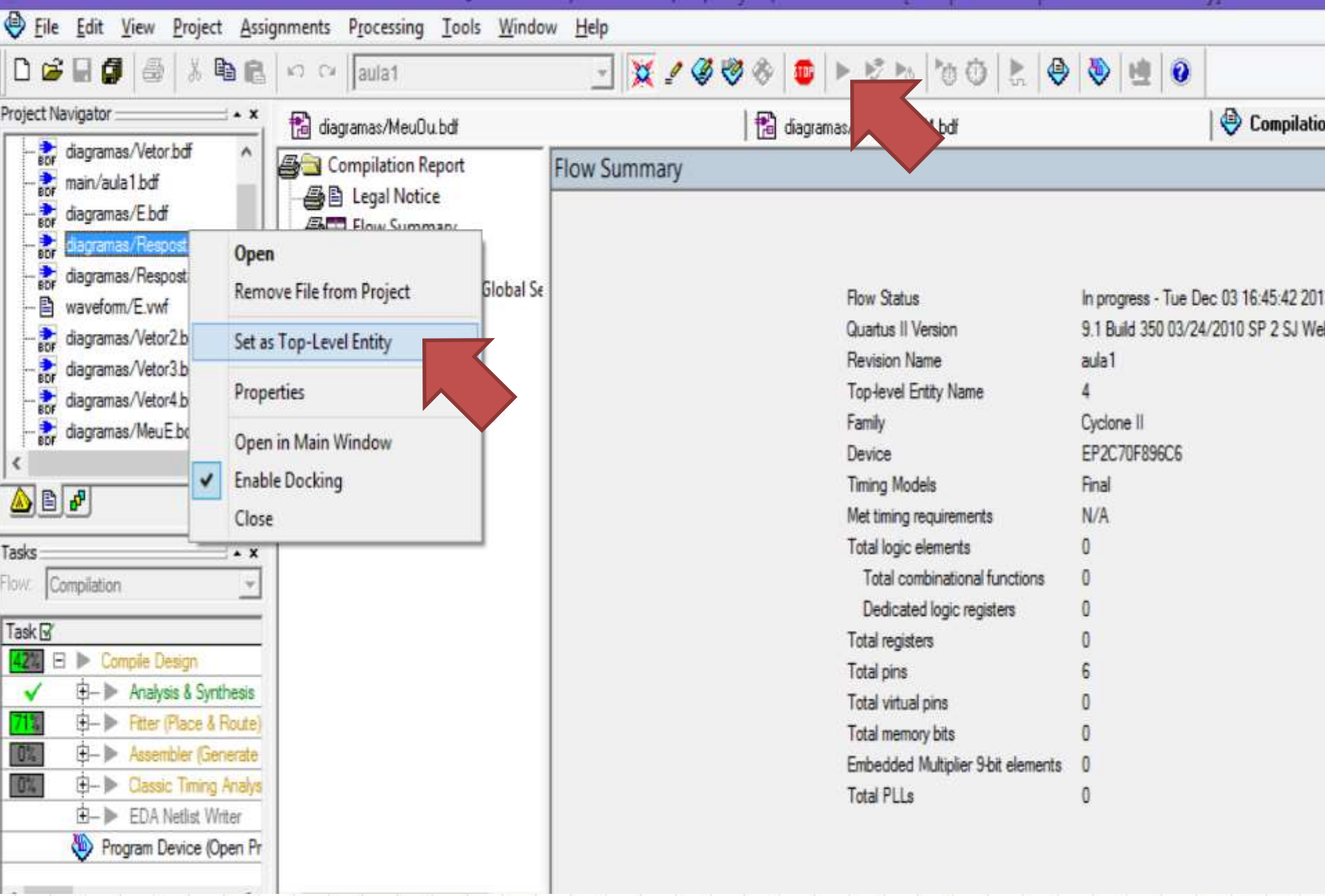
Compilar, debugar

(A V B)

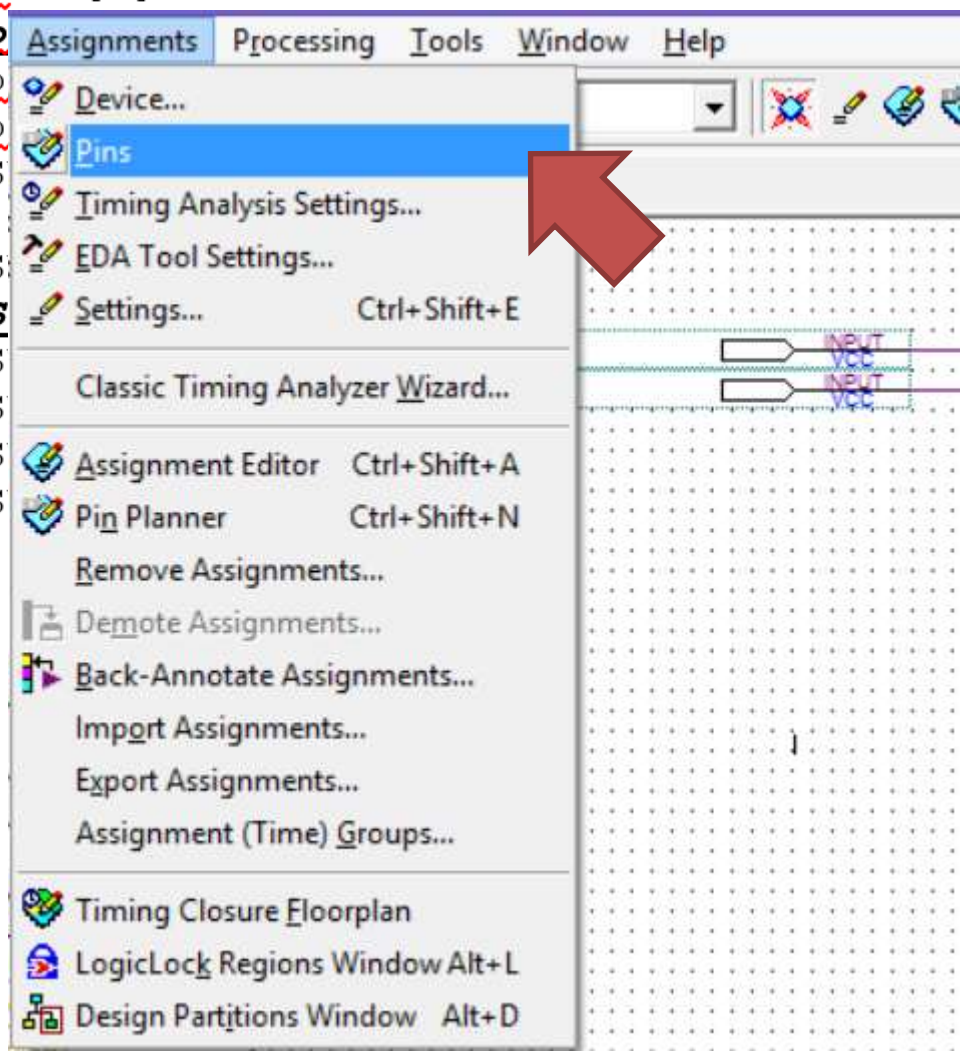


Parte 4: Pinagem


DC 9V
BLASTER
DEVICE
HOST
MIC
LINEIN
LINEOUT
VIDEO IN
VGA
Sumlink
ST - J0012
China M 0515
ETHERNET
RS232
PS/2 KB
LCD MODULE 16X2
ALTERA
Cyclone II
EP2C35F672C6
K AAB9T0531A
KOREA
SDRAM 8MB
SRAM 512KB
FLASH 1MB
SD CARD
IRDA
EXT CLK
RUN
PROG
©ALTERA
www.altera.com
DE2
ALTERA
HEX7
HEX6
HEX5
HEX4
HEX3
HEX2
HEX1
HEX0
LEDR17
LEDR16
LEDR15
LEDR14
LEDR13
LEDR12
LEDR11
LEDR10
LEDR9
LEDR8
LEDR7
LEDR6
LEDR5
LEDR4
LEDR3
LEDR2
LEDR1
LEDR0
LEDG7
LEDG6
LEDG5
LEDG4
LEDG3
LEDG2
LEDG1
LEDG0
SW17
SW16
SW15
SW14
SW13
SW12
SW11
SW10
SW9
SW8
SW7
SW6
SW5
SW4
SW3
SW2
SW1
SW0
KEY3
KEY2
KEY1
KEY0


File Edit View Project Assignments Processing Tools Window Help
aula1
Project Navigator
diagramas/Vetor.bdf
main/aula1.bdf
diagramas/E.bdf
diagramas/Respost
diagramas/Respost
waveform/E.vwf
diagramas/Vetor2.b
diagramas/Vetor3.b
diagramas/Vetor4.b
diagramas/MeuE.bc
Open
Remove File from Project
Set as Top-Level Entity
Properties
Open in Main Window
Enable Docking
Close
Tasks
Flow: Compilation
Task
42% Compile Design
Analysis & Synthesis
71% Fitter (Place & Route)
0% Assembler (Generate
0% Classic Timing Analys
EDA Netlist Writer
Program Device (Open Pr
diagramas/MeuOu.bdf
Compilation Report
Legal Notice
Flow Summary
Global Se
Flow Summary
Flow Status In progress - Tue Dec 03 16:45:42 201
Quartus II Version 9.1 Build 350 03/24/2010 SP 2 SJ We
Revision Name aula1
Top-level Entity Name 4
Family Cyclone II
Device EP2C70F896C6
Timing Models Final
Met timing requirements N/A
Total logic elements 0
Total combinational functions 0
Dedicated logic registers 0
Total registers 0
Total pins 6
Total virtual pins 0
Total memory bits 0
Embedded Multiplier 9-bit elements 0
Total PLLs 0

```
set_location_assignment PIN_AA23 -to SW[0]
set_location_assignment PIN_AB26 -to SW[1]
set_location_assignment PIN_AB25 -to SW[2]
set_location_assignment PIN_AC27 -to SW[3]
set_location_assignment PIN_AC26 -to SW[4]
set_location_assignment PIN_AC24 -to SW[5]
set_location_assignment PIN_AC23 -to SW[6]
set_location_assignment PIN_AD25 -to
set_location_assignment PIN_AD24 -to
set_location_assignment PIN_AE27 -to
set_location_assignment PIN_W5 -to S
set_location_assignment PIN_V10 -to
set_location_assignment PIN_U9 -to S
set_location_assignment PIN_T9 -to S
set_location_assignment PIN_L5 -to S
set_location_assignment PIN_L4 -to S
set_location_assignment PIN_L7 -to S
set_location_assignment PIN_L8 -to S
```



Quartus II - E:/Downloads/SD/Projeto/aula1 - aula1 - [Pin Planner]

Edit View Processing Tools Window

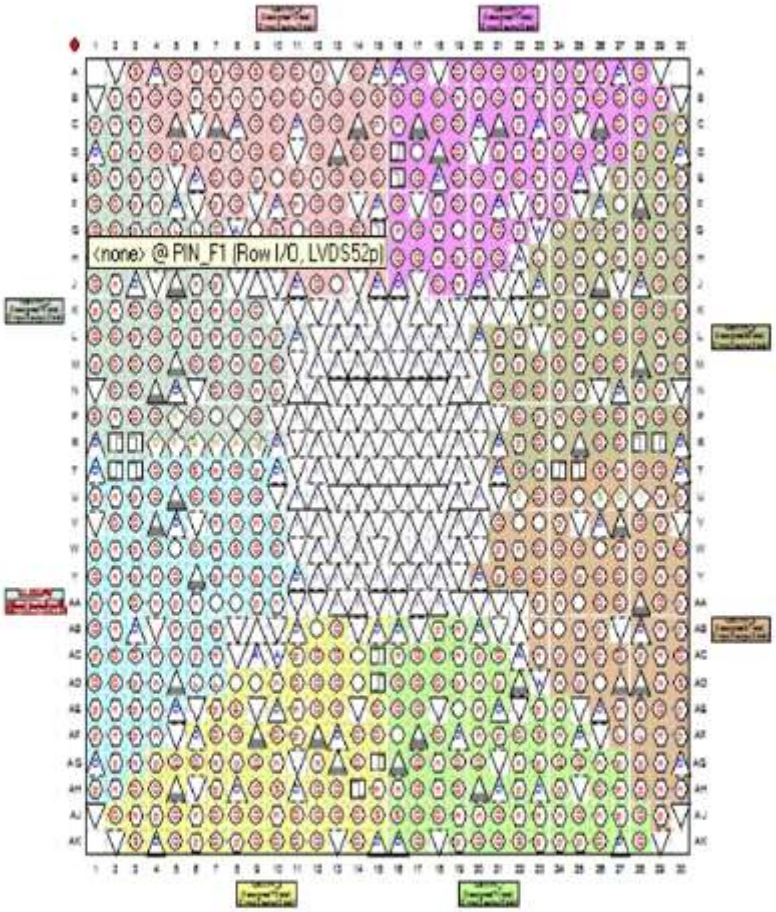
Groups

Named:

Node Name	D
<<new node>>	

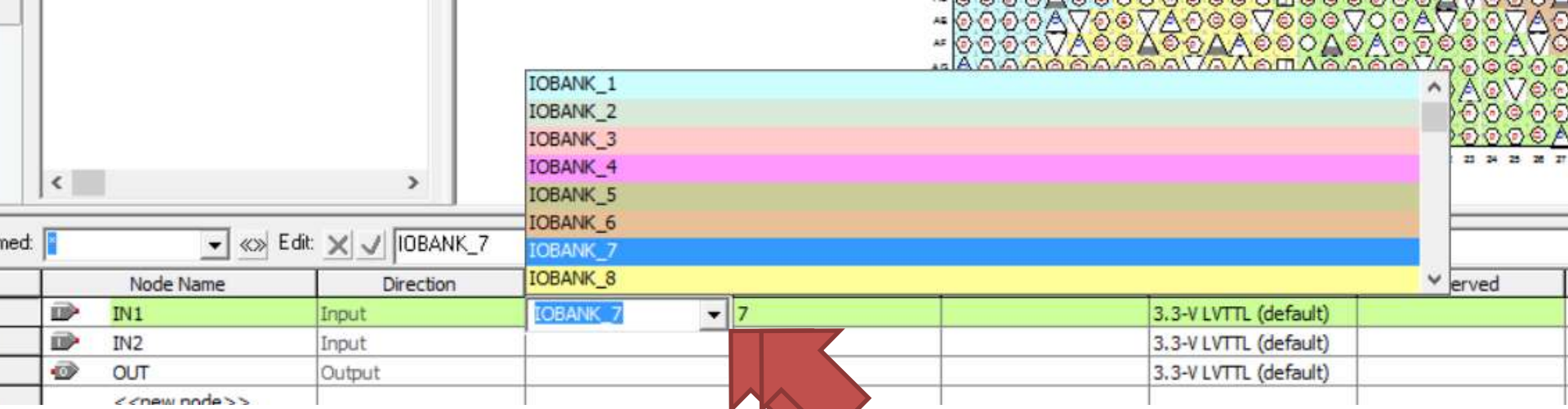
Top View - Wire Bond

Cyclone II - EP2C70F896C6



Named: Edit: Filter: Pins: all

	Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved
1	IN1	Input	IOBANK_1	1		3.3-V LVTTL (default)	
2	IN2	Input				3.3-V LVTTL (default)	
3	OUT	Output				3.3-V LVTTL (default)	
4	<<new node>>						



Ou digitando

```
location assignment PIN_AA23 -to SW[0]
location assignment PIN_AB26 -to SW[1]
location assignment PIN_AB25 -to SW[2]
location assignment PIN_AC27 -to SW[3]
location assignment PIN_AC26 -to SW[4]
location assignment PIN_AC24 -to SW[5]
location assignment PIN_AC23 -to SW[6]
location assignment PIN_AD25 -to SW[7]
location assignment PIN_AD24 -to SW[8]
location assignment PIN_AE27 -to SW[9]
location assignment PIN_W5 -to SW[10]
location assignment PIN_V10 -to SW[11]
location assignment PIN_U9 -to SW[12]
location assignment PIN_T9 -to SW[13]
location assignment PIN_L5 -to SW[14]
location assignment PIN_L4 -to SW[15]
location assignment PIN_L7 -to SW[16]
location assignment PIN_L8 -to SW[17]
```

```
set location assignment PIN_P30 -to GPIO_1[31
set location assignment PIN_W27 -to LEDG[0]
set location assignment PIN_W25 -to LEDG[1]
set location assignment PIN_W23 -to LEDG[2]
set location assignment PIN_Y27 -to LEDG[3]
set location assignment PIN_Y24 -to LEDG[4]
set location assignment PIN_Y23 -to LEDG[5]
set location assignment PIN_AA27 -to LEDG[6]
set location assignment PIN_AA24 -to LEDG[7]
set location assignment PIN_AC14 -to LEDG[8]
set location assignment PIN_AJ6 -to LEDR[0]
set location assignment PIN_AK5 -to LEDR[1]
set location assignment PIN_AJ5 -to LEDR[2]
set location assignment PIN_AJ4 -to LEDR[3]
set location assignment PIN_AK3 -to LEDR[4]
set location assignment PIN_AH4 -to LEDR[5]
set location assignment PIN_AJ3 -to LEDR[6]
set location assignment PIN_AJ2 -to LEDR[7]
set location assignment PIN_AH3 -to LEDR[8]
set location assignment PIN_AD14 -to LEDR[9]
set location assignment PIN_AC13 -to LEDR[10]
set location assignment PIN_AB13 -to LEDR[11]
```

amed: Edit: PIN_W27

	Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved
	IN1	Input	PIN_AA23	6	B6_N2	3.3-V LVTTL (default)	
	IN2	Input	PIN_AB26	6	B6_N2	3.3-V LVTTL (default)	
	OUT	Output	PIN_W27	6	B6_N1	3.3-V LVTTL (default)	
	<<new node>>						

```
location assignment PIN_AA23 -to SW[0]
location assignment PIN_AB26 -to SW[1]
location assignment PIN_AB25 -to SW[2]
location assignment PIN_AC27 -to SW[3]
location assignment PIN_AC26 -to SW[4]
location assignment PIN_AC24 -to SW[5]
location assignment PIN_AC23 -to SW[6]
location assignment PIN_AD25 -to SW[7]
location assignment PIN_AD24 -to SW[8]
location assignment PIN_AE27 -to SW[9]
location assignment PIN_W5 -to SW[10]
location assignment PIN_V10 -to SW[11]
location assignment PIN_U9 -to SW[12]
location assignment PIN_T9 -to SW[13]
location assignment PIN_L5 -to SW[14]
location assignment PIN_L4 -to SW[15]
location assignment PIN_L7 -to SW[16]
location assignment PIN_L8 -to SW[17]
```

```
set location assignment PIN_P30 -to GPIO_1[31
set location assignment PIN_W27 -to LEDG[0]
set location assignment PIN_W25 -to LEDG[1]
set location assignment PIN_W23 -to LEDG[2]
set location assignment PIN_Y27 -to LEDG[3]
set location assignment PIN_Y24 -to LEDG[4]
set location assignment PIN_Y23 -to LEDG[5]
set location assignment PIN_AA27 -to LEDG[6]
set location assignment PIN_AA24 -to LEDG[7]
set location assignment PIN_AC14 -to LEDG[8]
set location assignment PIN_AJ6 -to LEDR[0]
set location assignment PIN_AK5 -to LEDR[1]
set location assignment PIN_AJ5 -to LEDR[2]
set location assignment PIN_AJ4 -to LEDR[3]
set location assignment PIN_AK3 -to LEDR[4]
set location assignment PIN_AH4 -to LEDR[5]
set location assignment PIN_AJ3 -to LEDR[6]
set location assignment PIN_AJ2 -to LEDR[7]
set location assignment PIN_AH3 -to LEDR[8]
set location assignment PIN_AD14 -to LEDR[9]
set location assignment PIN_AC13 -to LEDR[10]
set location assignment PIN_AB13 -to LEDR[11]
```

Quartus II - E:/Downloads/SD/Projeto/aula1 - aula1 - [Pin Planner]

Edit View Processing Tools Window

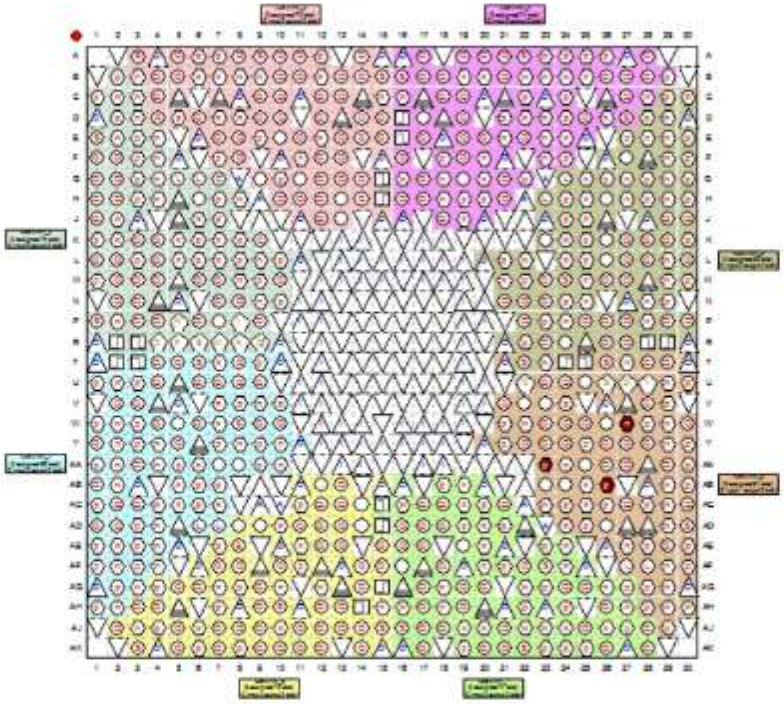
Groups

Named:

Node Name	D
<<new node>>	

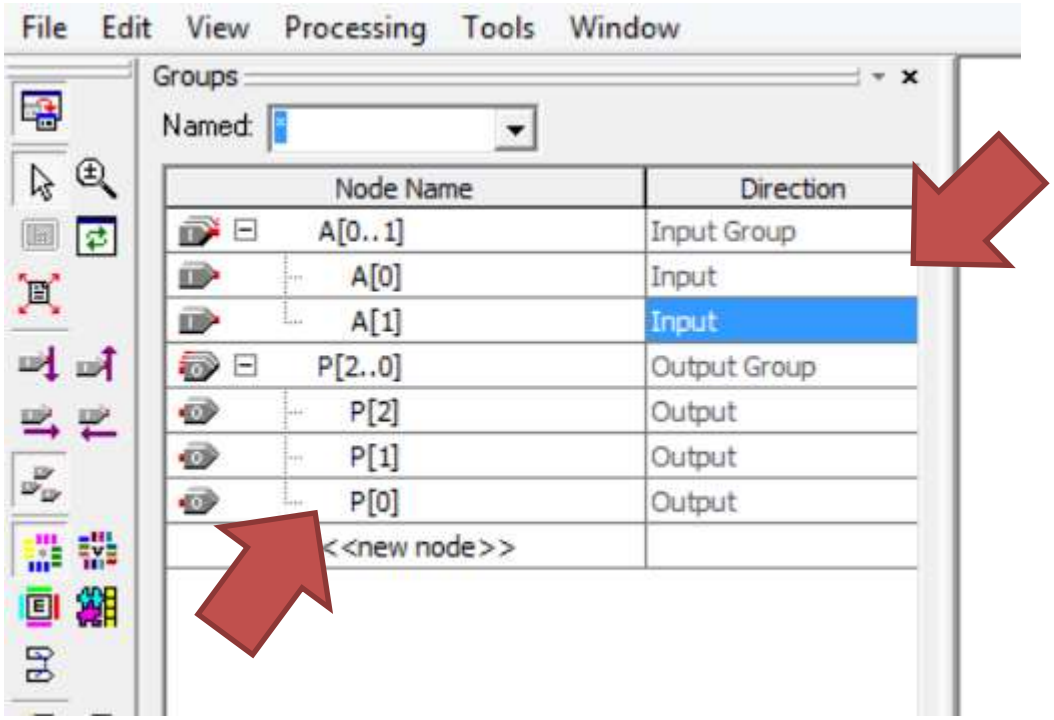
Top View - Wire Bond

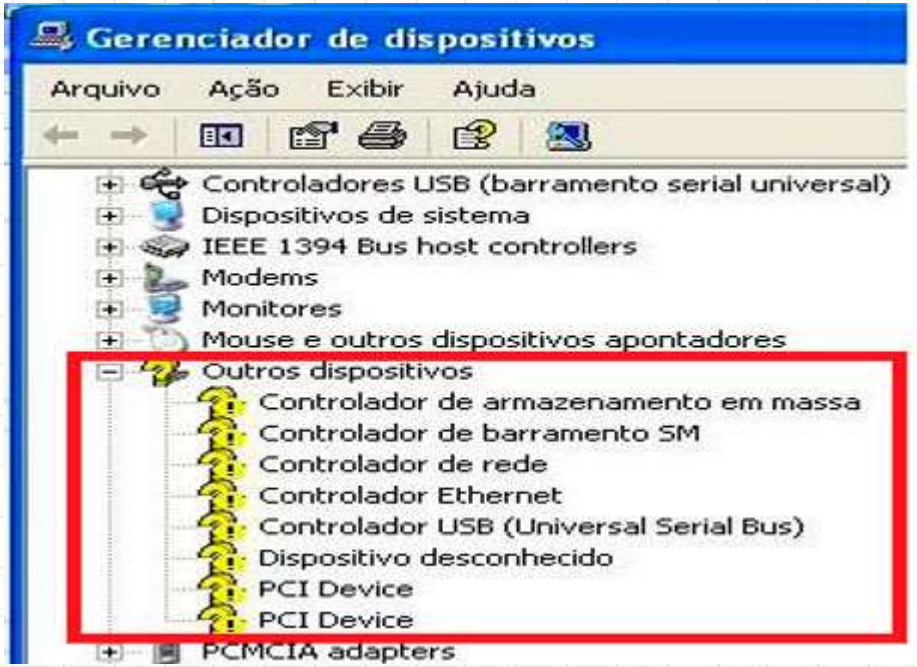
Cyclone II - EP2C70F896C6



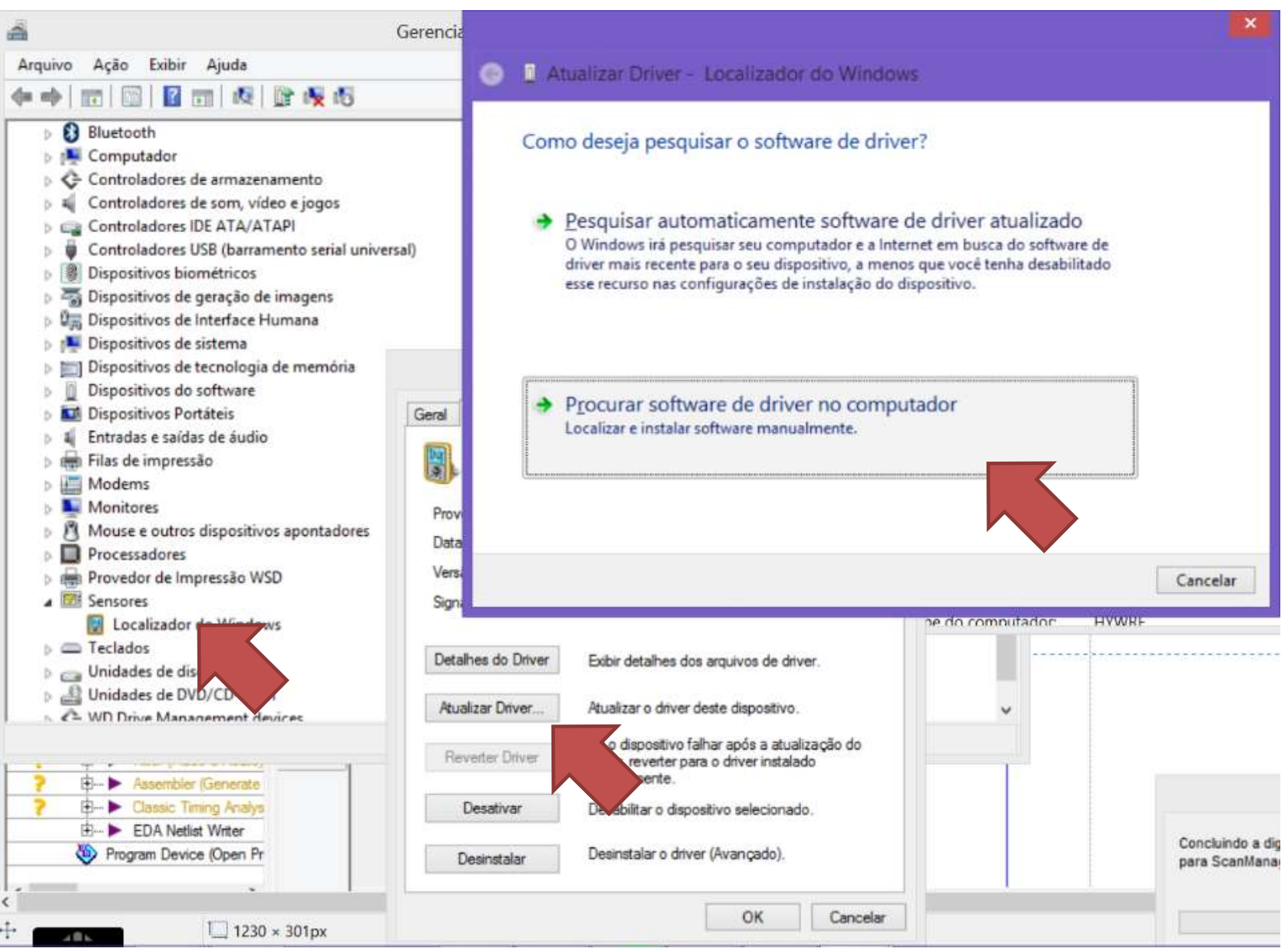
Named: Edit: PIN_W27 Filter: Pins: all

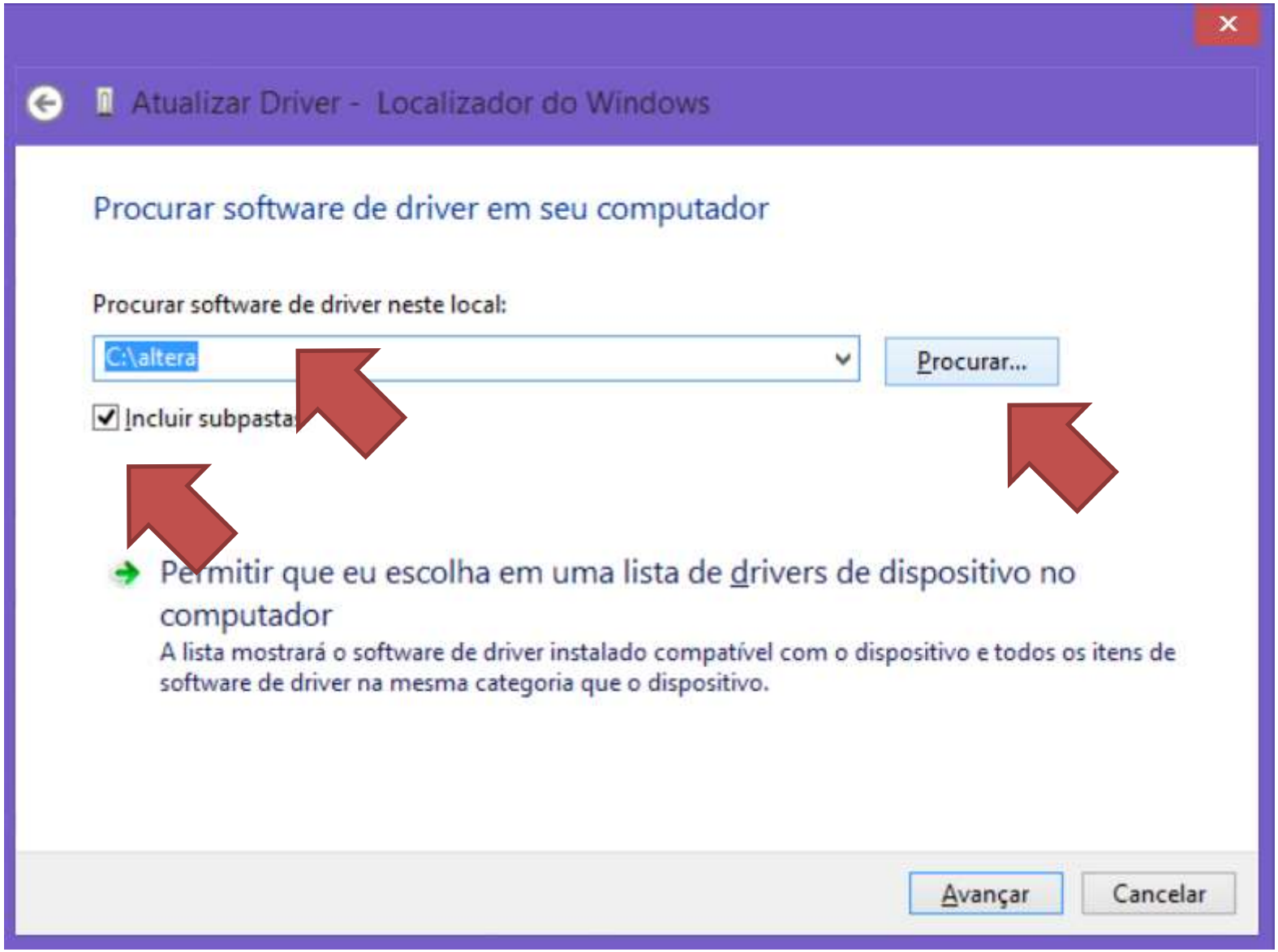
	Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved
1	IN1	Input	PIN_AA23	6	B6_N2	3.3-V LVTTL (default)	
2	IN2	Input	PIN_AB26	6	B6_N2	3.3-V LVTTL (default)	
3	OUT	Output	PIN_W27	6	B6_N1	3.3-V LVTTL (default)	
4	<<new node>>						


File
Edit
View
Processing
Tools
Window
Groups
Named:
Node Name
Direction
A[0..1]
Input Group
A[0]
Input
A[1]
Input
P[2..0]
Output Group
P[2]
Output
P[1]
Output
P[0]
Output
<<new node>>

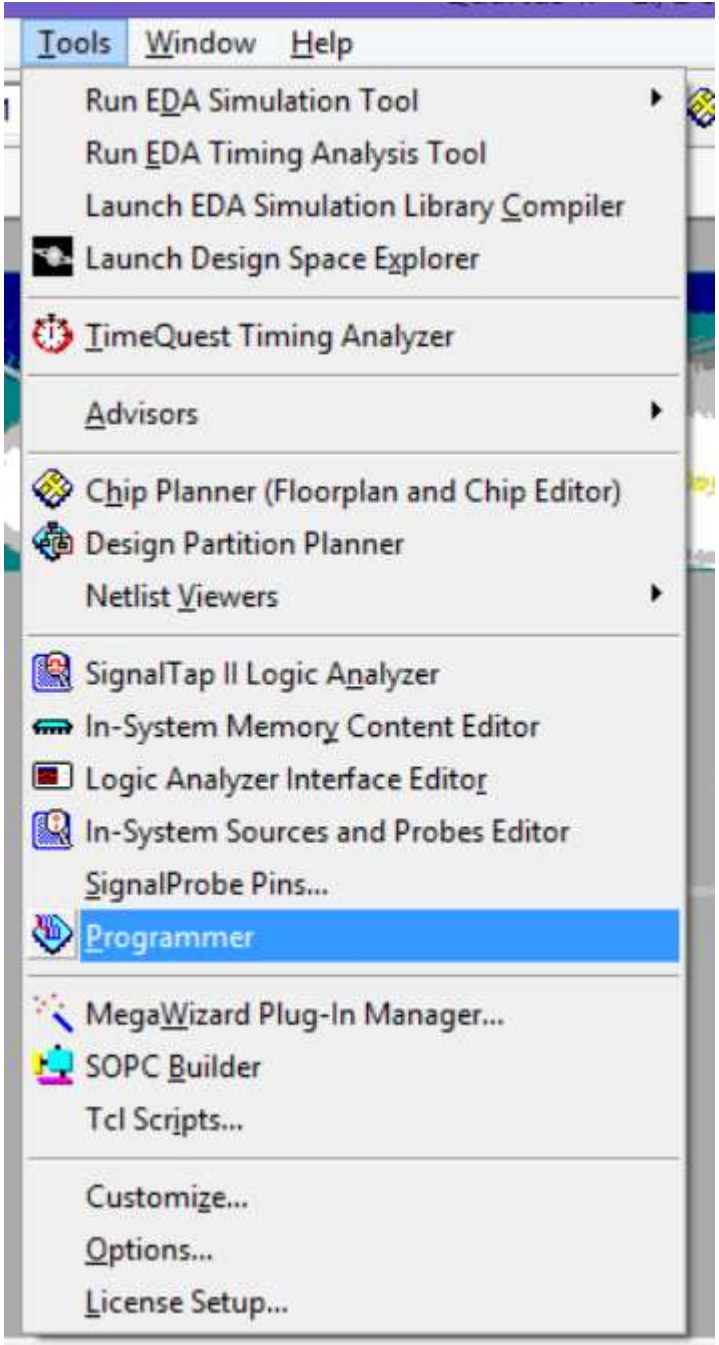


Parte 5: Instalando Placa


Gerenciador de Dispositivos
Arquivo Ação Exibir Ajuda
Bluetooth
Computador
Controladores de armazenamento
Controladores de som, vídeo e jogos
Controladores IDE ATA/ATAPI
Controladores USB (barramento serial universal)
Dispositivos biométricos
Dispositivos de geração de imagens
Dispositivos de Interface Humana
Dispositivos de sistema
Dispositivos de tecnologia de memória
Dispositivos do software
Dispositivos Portáteis
Entradas e saídas de áudio
Filas de impressão
Modems
Monitores
Mouse e outros dispositivos apontadores
Processadores
Provedor de Impressão WSD
Sensores
Localizador do Windows
Teclados
Unidades de DVD/CD
Assembler (Generate
Classic Timing Analys
EDA Netlist Writer
Program Device (Open Pr
Atualizar Driver - Localizador do Windows
Como deseja pesquisar o software de driver?
Pesquisar automaticamente software de driver atualizado
O Windows irá pesquisar seu computador e a Internet em busca do software de driver mais recente para o seu dispositivo, a menos que você tenha desabilitado esse recurso nas configurações de instalação do dispositivo.
Procurar software de driver no computador
Localizar e instalar software manualmente.
Cancelar
Geral
Detalhes do Driver
Exibir detalhes dos arquivos de driver.
Atualizar Driver...
Atualizar o driver deste dispositivo.
Reverter Driver
Desativar
Desinstalar
Desinstalar o driver (Avançado).
OK
Cancelar
1230 × 301px


Atualizar Driver - Localizador do Windows
Procurar software de driver em seu computador
Procurar software de driver neste local:
C:\altera
Procurar...
Incluir subpastas
Permitir que eu escolha em uma lista de drivers de dispositivo no computador
A lista mostrará o software de driver instalado compatível com o dispositivo e todos os itens de software de driver na mesma categoria que o dispositivo.
Avançar
Cancelar

Parte 6:
Upload (Programming)



1. Compilou o projeto
2. Salvou e fechou todos os arquivos
3.

Quartus II - E:/Downloads/SD/Projeto/aula1 - aula1

File Edit View Project Assignments Processing Tools Window Help

aula1

Project Navigator

- diagramas/Vetor.bdf
- main/aula1.bdf
- diagramas/E.bdf
- diagramas/Respostas/4.bd
- diagramas/Respostas/3.bd
- waveform/E.vwf
- diagramas/Vetor2.bdf
- diagramas/Vetor3.bdf
- diagramas/Vetor4.bdf
- diagramas/MeuE.bdf

Tasks

Flow: Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate
- Classic Timing Analys
- EDA Netlist Writer
- Program Device (Open Pr

ALTERA

QUARTUS II

Version 9.1

View Quartus II Information

Documentation

Type	Message
	Info: Longest tpd from source pin "A[0]" to destination pin "Sinal" is 4.820 ns
	Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 0 warnings
	Info: Quartus II Full Compilation was successful. 0 errors, 17 warnings

System (112) Processing (66) Extra Info Info (56) Warning (9) Critical Warning (1) Error Suppressed (6) Flag

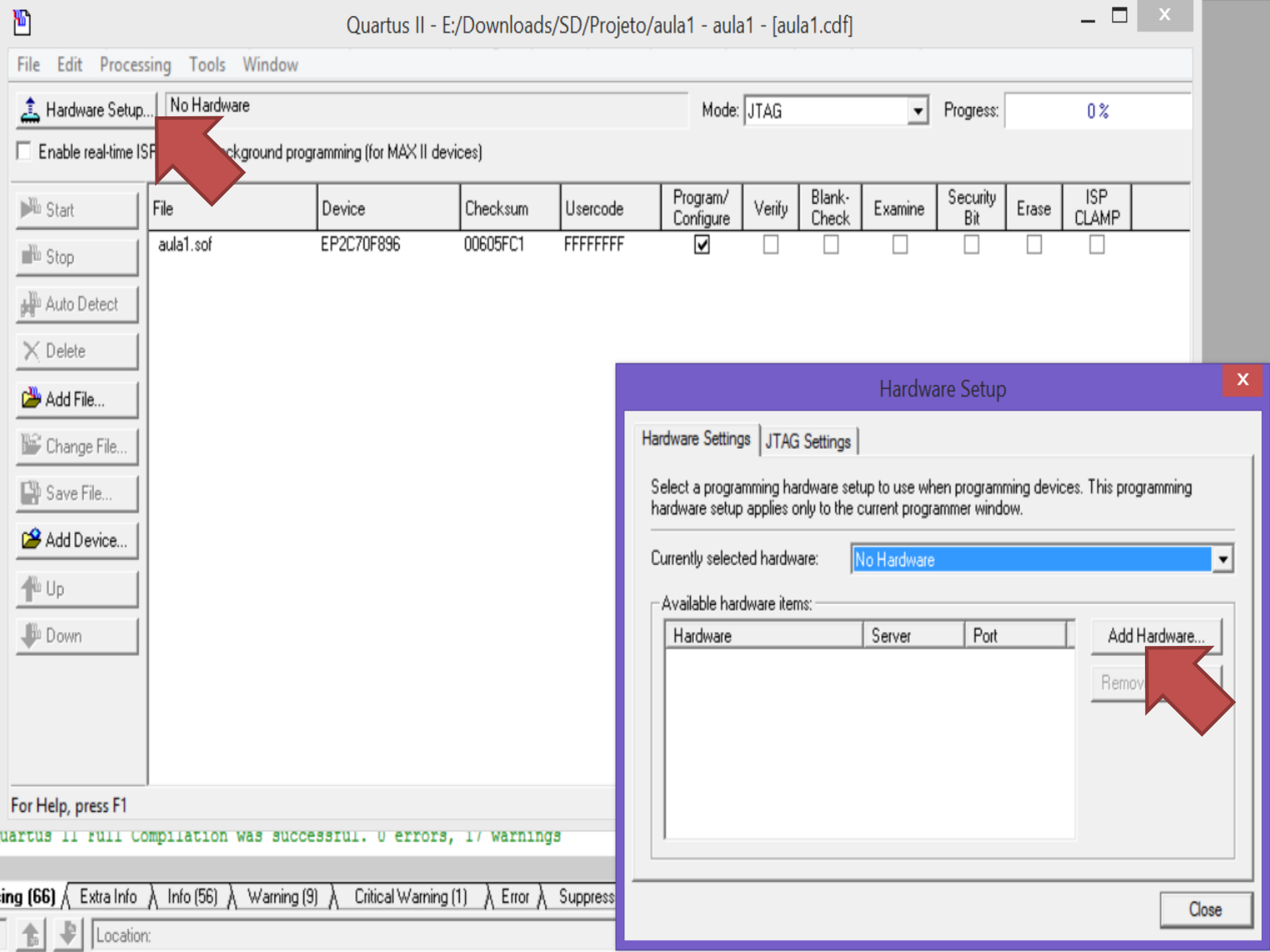
Message: 0 of 141

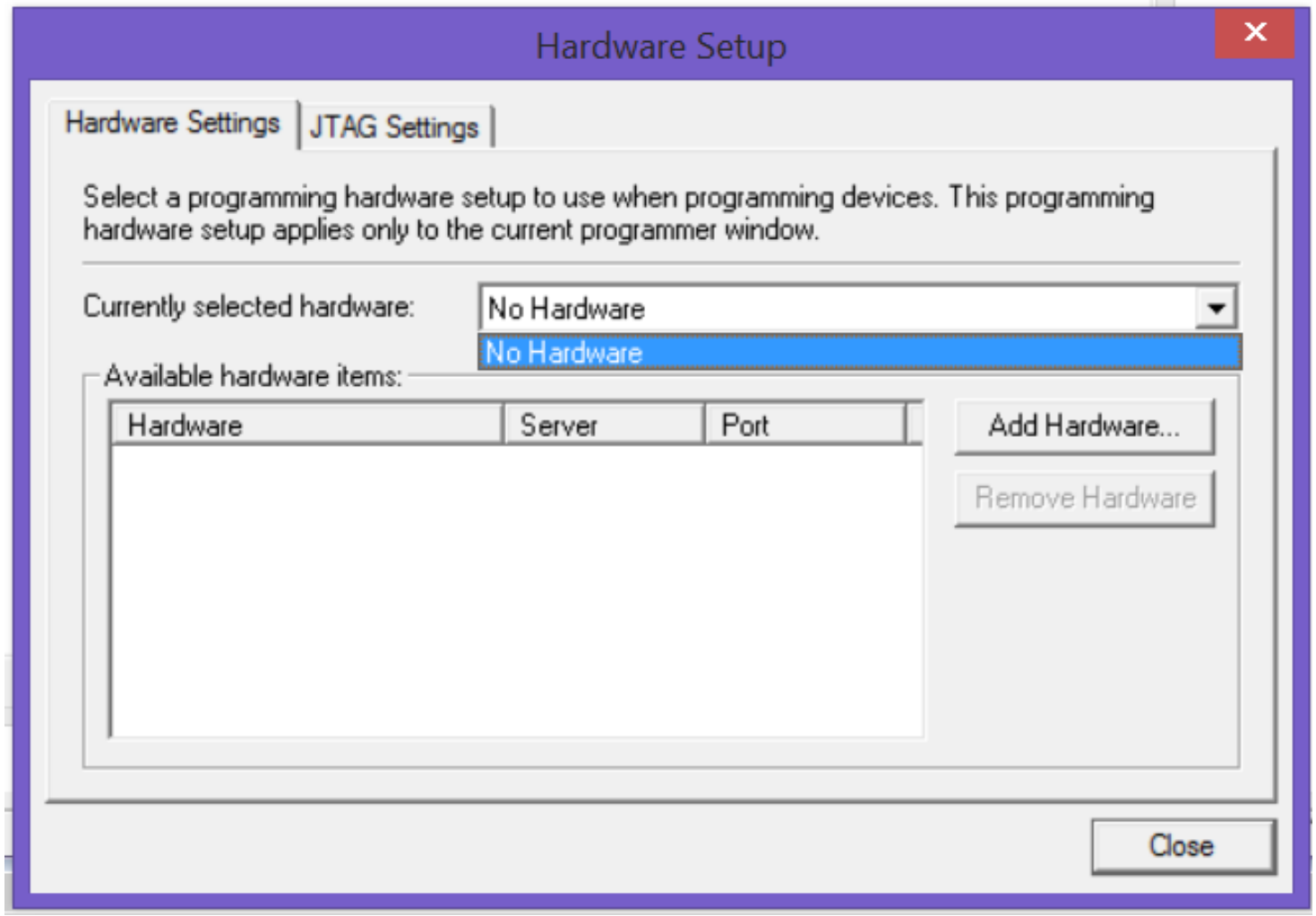
Location:

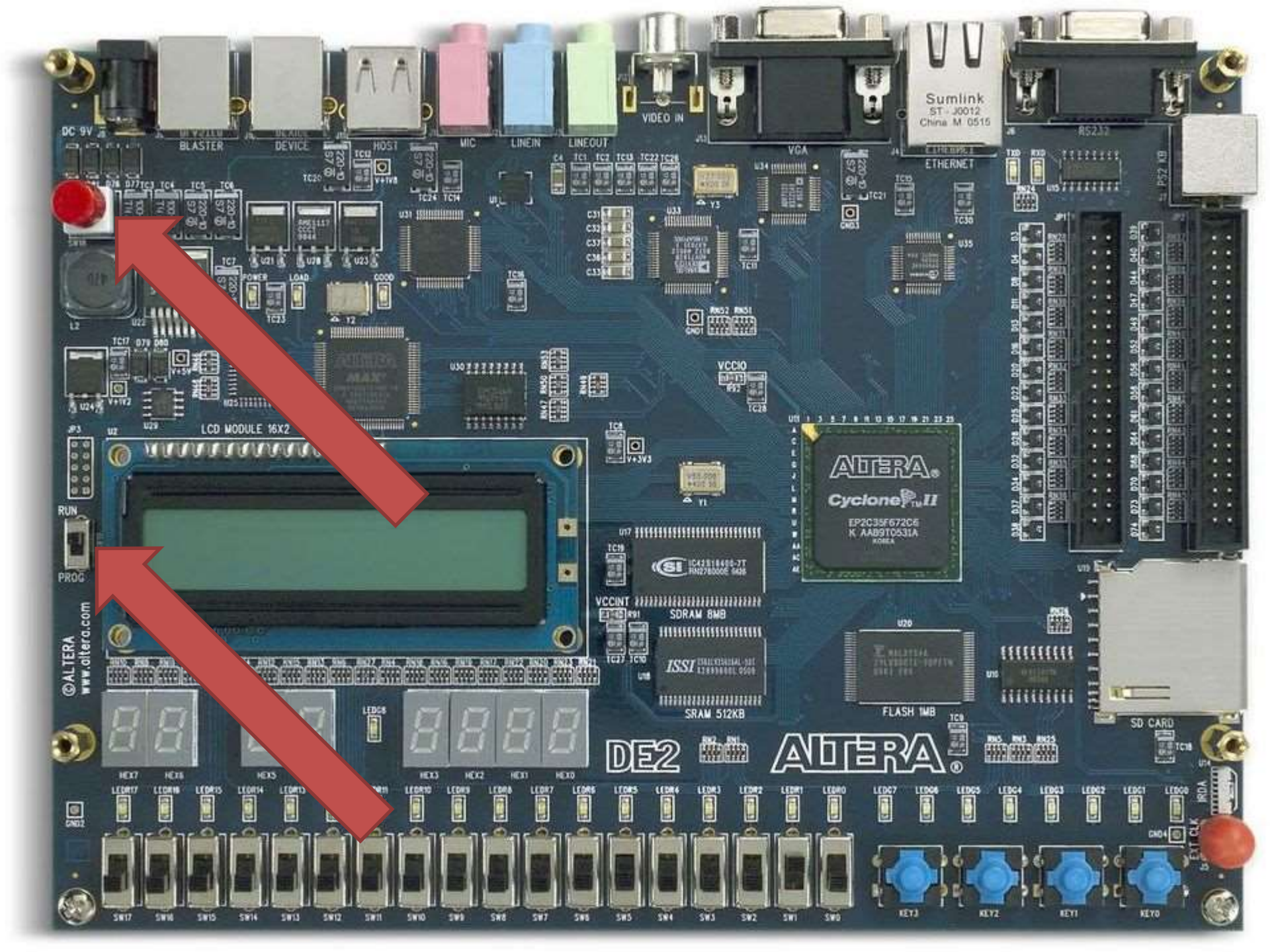
Locate

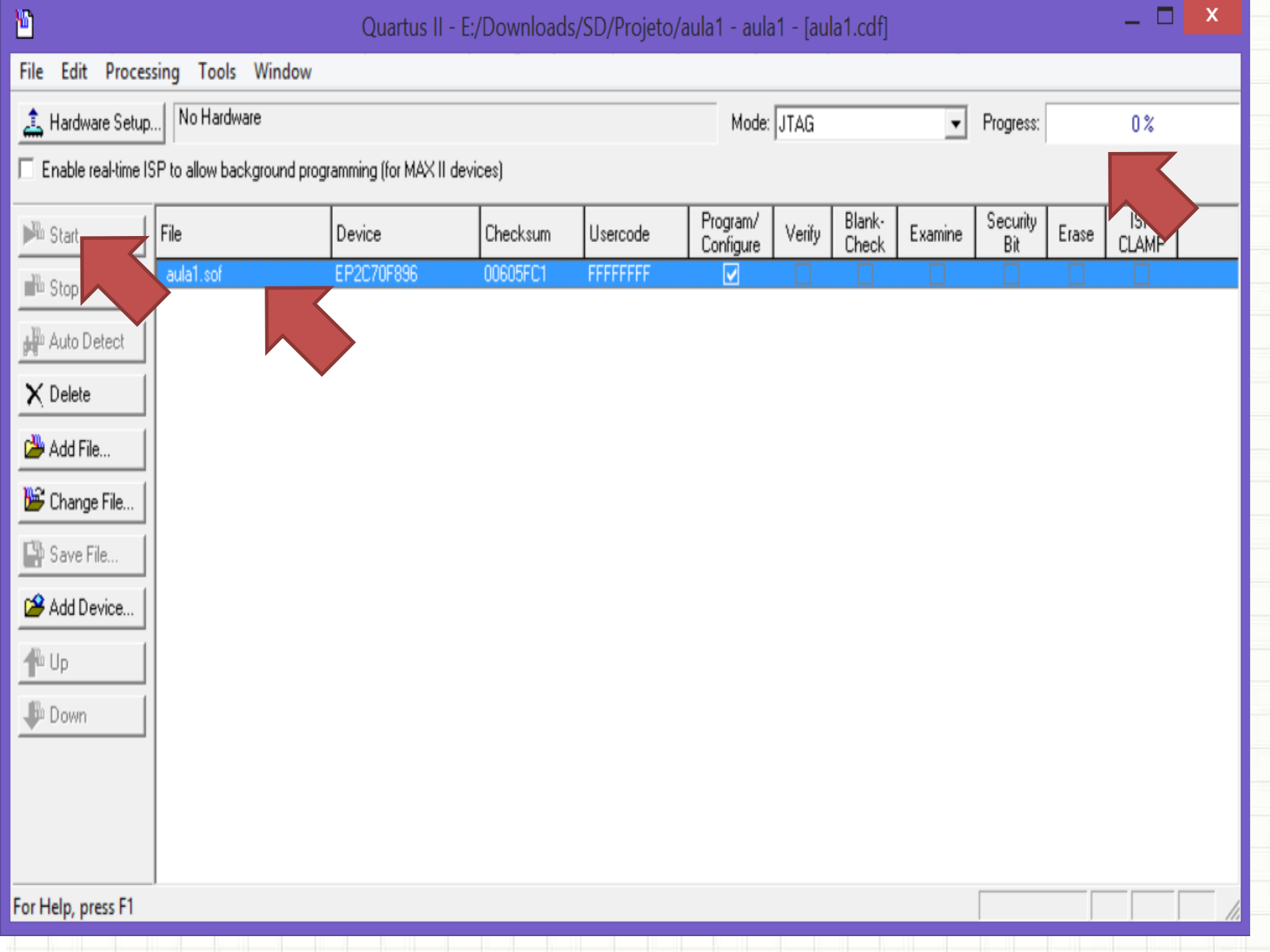
Messages

Idle


Quartus II - E:/Downloads/SD/Projeto/aula1 - aula1 - [aula1.cdf]
File Edit Processing Tools Window
Hardware Setup...
No Hardware
Mode: JTAG
Progress: 0 %
Enable real-time ISP
ckground programming (for MAX II devices)
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File...
Add Device...
Up
Down
File
Device
Checksum
Usercode
Program/ Configure
Verify
Blank-Check
Examine
Security Bit
Erase
ISP CLAMP
aula1.sof
EP2C70F896
00605FC1
FFFFFFFF
For Help, press F1
uartus II Full Compilation was successful. 0 errors, 17 warnings
ing (66)
Extra Info
Info (56)
Warning (9)
Critical Warning (1)
Error
Suppress
Location:
Hardware Setup
Hardware Settings
JTAG Settings
Select a programming hardware setup to use when programming devices. This programming hardware setup applies only to the current programmer window.
Currently selected hardware:
No Hardware
Available hardware items:
Hardware
Server
Port
Add Hardware...
Remov
Close


Hardware Setup
Hardware Settings
JTAG Settings
Select a programming hardware setup to use when programming devices. This programming hardware setup applies only to the current programmer window.
Currently selected hardware:
No Hardware
No Hardware
Available hardware items:
Hardware
Server
Port
Add Hardware...
Remove Hardware
Close


DC 9V
BLASTER
DEVICE
HOST
MIC
LINEIN
LINEOUT
VIDEO IN
VGA
Sumlink
ST - J0012
China M 0515
ETHERNET
RS232
PS/2 KB
LCD MODULE 16X2
RUN
PROG
©ALTERA
www.altera.com
ALTERA
Cyclone II
EP2C35F672C6
K AAB9T0531A
KOREA
VCCIO
VCCINT
SDRAM 8MB
SRAM 512KB
FLASH 1MB
SD CARD
DE2
ALTERA
IRDA
EXT CLK
HEX7
HEX6
HEX5
HEX4
HEX3
HEX2
HEX1
HEX0
SW17
SW16
SW15
SW14
SW13
SW12
SW11
SW10
SW9
SW8
SW7
SW6
SW5
SW4
SW3
SW2
SW1
SW0
KEY3
KEY2
KEY1
KEY0


Quartus II - E:/Downloads/SD/Projeto/aula1 - aula1 - [aula1.cdf]
File Edit Processing Tools Window
Hardware Setup...
No Hardware
Mode: JTAG
Progress:
0 %
Enable real-time ISP to allow background programming (for MAX II devices)
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File...
Add Device...
Up
Down
File
Device
Checksum
Usercode
Program/ Configure
Verify
Blank-Check
Examine
Security Bit
Erase
CLAMP
aula1.sof
EP2C70F896
00605FC1
FFFFFFFF
For Help, press F1

Quartus II - E:/Downloads/SD/Projeto/aula1 - aula1

File Edit View Project Assignments Processing Tools Window Help

aula1

Project Navigator

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- diagramas/Vetor2.bdf
- diagramas/Vetor3.bdf
- diagramas/Vetor4.bdf
- diagramas/MeuE.bdf

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Flow: Compilation

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QUARTUS II

Version 9.1

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Message: 0 of 141

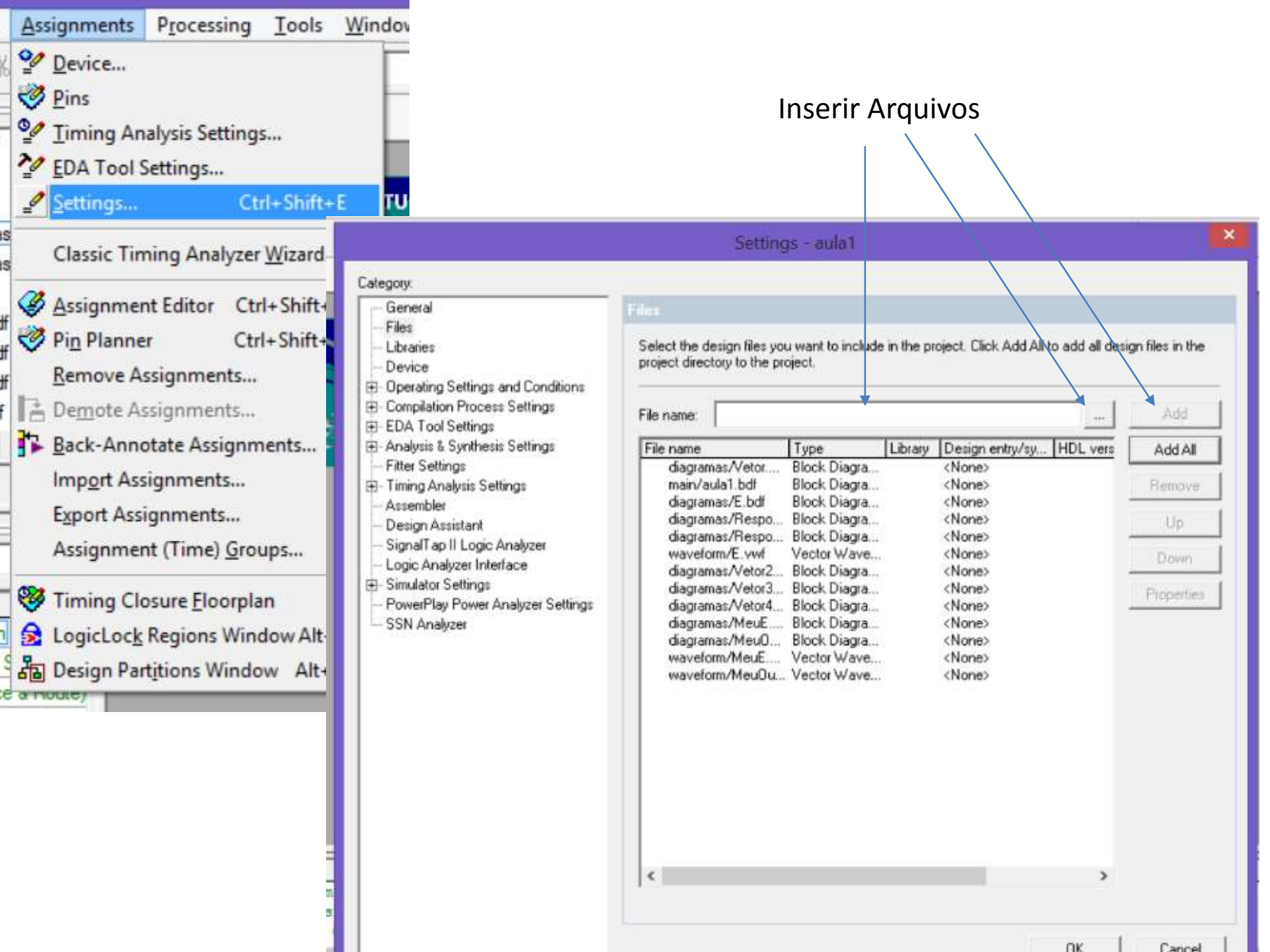
Location:

Locate

Messages

Idle

IMPORTANTE:
fechar projeto cada vez que for programar.


Assignments
Processing
Tools
Device...
Pins
Timing Analysis Settings...
EDA Tool Settings...
Settings... Ctrl+Shift+E
Classic Timing Analyzer Wizard
Assignment Editor Ctrl+Shift+
Pin Planner Ctrl+Shift+
Remove Assignments...
Demote Assignments...
Back-Annotate Assignments...
Import Assignments...
Export Assignments...
Assignment (Time) Groups...
Timing Closure Floorplan
LogicLock Regions Window Alt+
Design Partitions Window Alt+
Inserir Arquivos
Settings - aula1
Category:
General
Files
Libraries
Device
Operating Settings and Conditions
Compilation Process Settings
EDA Tool Settings
Analysis & Synthesis Settings
Fitter Settings
Timing Analysis Settings
Assembler
Design Assistant
SignalTap II Logic Analyzer
Logic Analyzer Interface
Simulator Settings
PowerPlay Power Analyzer Settings
SSN Analyzer
Files
Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project.
File name:
Add
Add All
Remove
Up
Down
Properties
File name
Type
Library
Design entry/sy...
HDL vers
diagramas/Vetor....
Block Diagra...
<None>
main/aula1.bdf
Block Diagra...
<None>
diagramas/E.bdf
Block Diagra...
<None>
diagramas/Respo...
Block Diagra...
<None>
diagramas/Respo...
Block Diagra...
<None>
waveform/E.vwf
Vector Wave...
<None>
diagramas/Vetor2...
Block Diagra...
<None>
diagramas/Vetor3...
Block Diagra...
<None>
diagramas/Vetor4...
Block Diagra...
<None>
diagramas/MeuE....
Block Diagra...
<None>
diagramas/Meu0...
Block Diagra...
<None>
waveform/MeuE....
Vector Wave...
<None>
waveform/Meu0u...
Vector Wave...
<None>
OK
Cancel

- Obrigado.